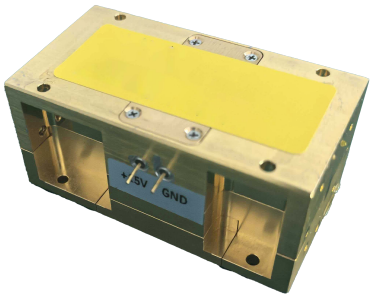
Standard Circuit

GPAm-4070

V-Band Power Amplifier Module，40-70GHz

Performance characteristics

- Frequency Range: 40GHz～70GHz
- Power Gain: 20dB
- Psat(CW): 24.5dBm
- PAE: 10%
- +15V@0.2 A（Quiescent）
- Dimensions: 3.33mm×1.45mm×0.05mm



Product Description

GPAm-4070 is a power amplifier die implemented with GaN HEMT transistors and fabricated on a 0.13 μm GaN power MMIC process. It operates across the 40 GHz to 70 GHz frequency band with power gain higher than 20 dB, typical Psat of 24.5 dBm and typical power-added efficiency (PAE) of 10% under continuous-wave (CW) operation. The die features backside via grounding and dual supply operation, with typical bias conditions of Vd = +15 V and Vg = -2.2 V.

DC Electrical Specifications（T_A= +25℃）

Parameter	Symbol	Min	Typ	Max	Unit
Operating Gate Voltage	Vg	-	-2.2	-	V
Operating Drain Voltage	Vd	12	15	18	V
Quiescent Drain Current	Id	-	200	-	mA
Dynamic Drain Current	Idd	-	-	260	mA
Quiescent Gate Current	Ig	-	-	0.1	mA
Dynamic Gate Current	Igg	-	-	1	mA

RF Electrical Specifications（T_A= +25℃，Vd = +15V，Vg = -2.2V）

Parameter	Symbol	Min	Typ	Max	Unit
Frequency Range	f	40～70			GHz
Psat	Psat	24.5	-	27.5	dBm
Power Gain	Gp	20	-	23	dB
Power Gain Flatness	△Gp	-	-	±1.5	dB
PAE	PAE	-	10	-	%
Linear Gain	Gain		30		dB
Linear Gain Flatness	△Gain			±5	dB
Input VSWR	VSWR(in)		3	5.5	-

Note:

1) All dies undergo 100% on-wafer DC test and 100% RF test.
2) Unless specified otherwise, all characteristic curves in this datasheet are measured under the following conditions: Vd=+15 V, Vg=-2.2 V, Pin=5 dBm, CW operation.

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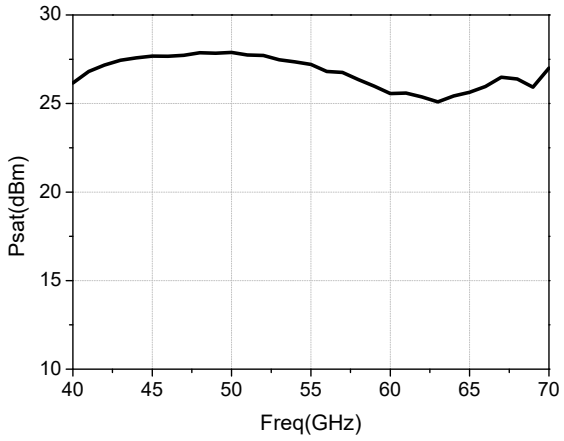
Absolute Maximum Ratings

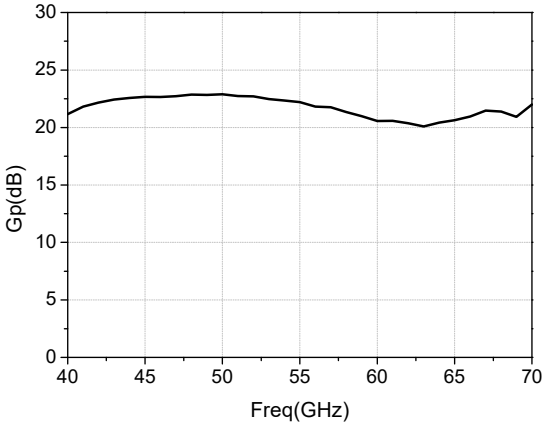
Parameter	Symbol	Value
Maximum Drain-Source Voltage	Vd	+20V
Minimum Gate-Source Voltage	Vg	-6V
Maximum CW Input RF Power（CW）	P_p	+12dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Maximum Operating Channel Temperature	T_{op}	+200℃
Load Mismatch Tolerance (Destruction-Proof)	Z_0	5：1

Typical Curves（Vd=+15V，Vg=-2.2V）

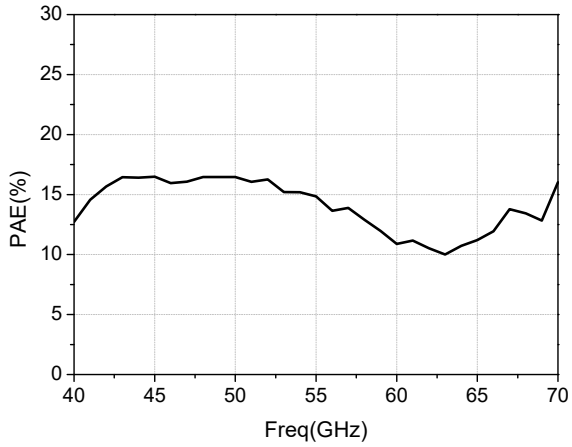
Psatvs. Frequency（P_{in}=5dBm）



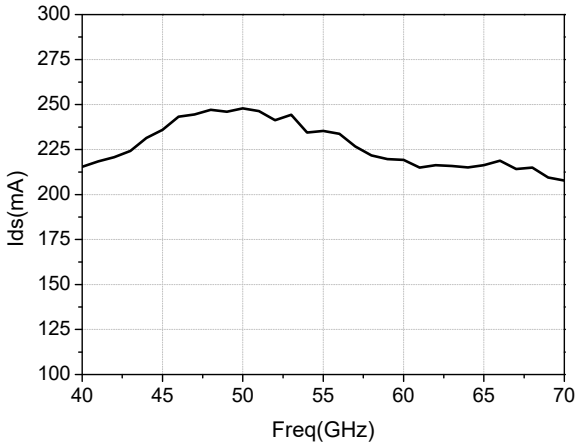
Powergainvs. Frequency（P_{in}=5dBm）



Efficiencyvs. Frequency（P_{in}=5dBm）



Dynamicdraincurrentvs. Frequency（P_{in}=5dBm）



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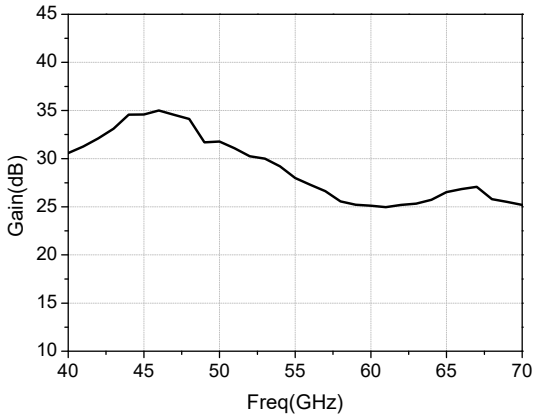
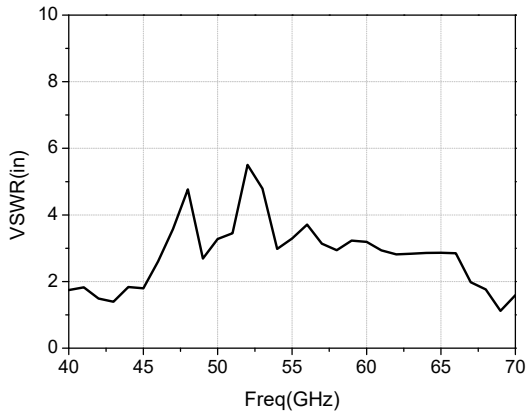
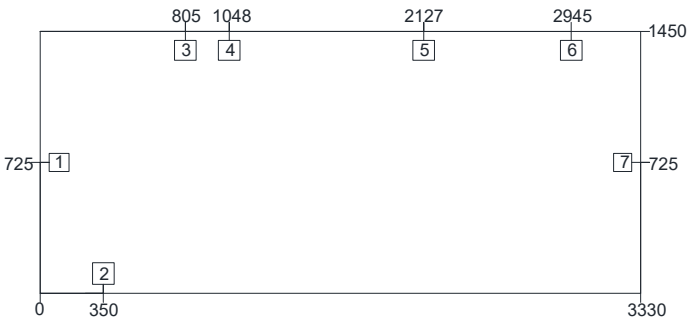
Smallsignalgainvs. Frequency（P_{in}=-10dBm)



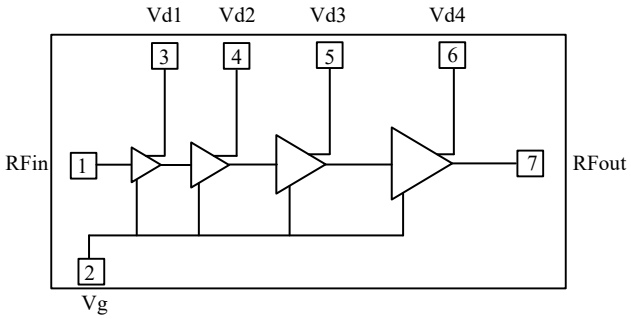
InputVSWRvs. Frequency（Pin=-10dBm）



Outline Dimensions & Bond Pad Layout Drawing



Block Diagram



Notes:

All dimensional units shown in the drawing are μm;
tolerance for outline dimensions is ±50 μm.

Bond Pad Layout

No.	Symbol	Function	Dimension
1	RFin	RF Input Bond Pad	110×100μm^2
2	Vg	Gate Bond Pad	120×120μm^2
3	Vd1	Drain Bond Pad	120×110μm^2
4	Vd2	Drain Bond Pad	120×110μm^2
5	Vd3	Drain Bond Pad	120×110μm^2
6	Vd4	Drain Bond Pad	120×110μm^2
7	RFout	RF Output Bond Pad	100×100μm^2

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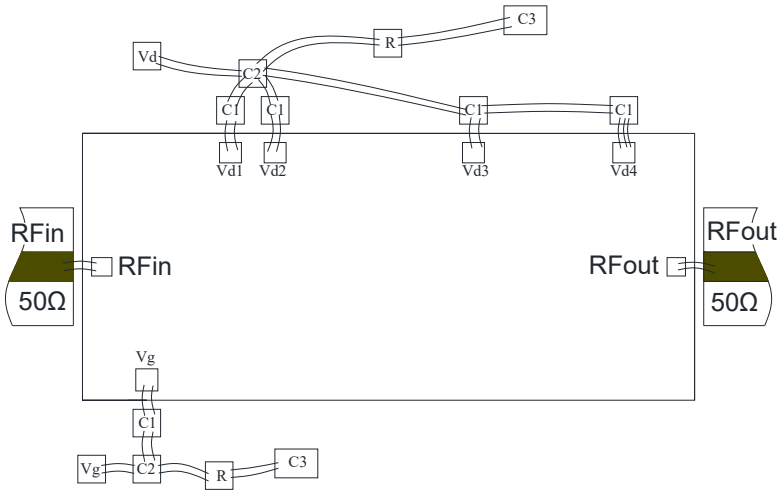
Recommended Assembly Schematic



Notes:

1) External component values: C1=100 pF, C2=1000 pF, C3=10000 pF. Resistor R is a 10 Ω die resistor, model NC6101C-E is recommended. All capacitors shall be placed as close to the die as possible, with a maximum distance not exceeding 300 μm.
2) The length of gold bonding wires for RF input and output shall be controlled within 300 μm ± 50 μm, kept as short as feasible.

Precautions

1) All MMIC dies shall be stored in a dry, clean nitrogen atmosphere.
2) The die substrate is made of brittle 6H-SiC. Handle with extreme care to prevent mechanical damage.
3) A passivation protection layer covers the die surface. Assembly must be performed in a clean environment to avoid excessive surface contamination.
4) The thermal expansion coefficient of the carrier material shall be close to that of 6H-SiC substrate (linear thermal expansion coefficient of 6H-SiC: 4.2×10 · ⁶/°C). Recommended carrier materials include CuMoCu, CuMo, CuW or other materials with superior heat dissipation performance.
5) Voids between the die and carrier substrate shall be eliminated during mounting. Ensure sufficient heat dissipation from the housing or carrier.
6) AuSn solder eutectic sintering is recommended. Sintering temperature shall not exceed 300°C with total sintering time ≤30 seconds. Avoid rapid temperature fluctuations; apply gradual temperature ramp-up and ramp-down profiles.
7) Gold bonding wires with diameter 25 μm ~ 30 μm are recommended. The chuck temperature of the wire bonder shall not exceed 250°C; minimize bonding duration and avoid abrupt temperature changes during bonding.
8) Power-up sequence: Apply gate bias first, then drain bias. Power-down sequence: Remove drain bias first, then gate bias.
9) Strict ESD protection must be implemented during all handling and assembly steps. Wear grounded ESD wrist straps, and ensure proper grounding for sintering and wire bonding equipment.
10) Contact your supplier for technical support if any problems occur.

This device is sensitive to electrostatic discharge. Strict ESD precautions are required during handling.

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