Standard Circuit

GLA-4775

Low Noise Amplifier，47-75GHz

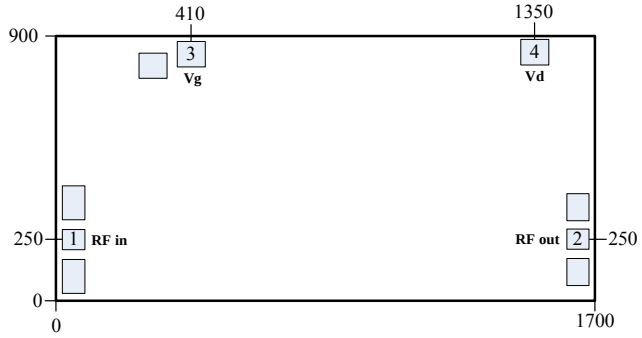
Performance characteristics

- ✧ Frequency range: 47GHz~75GHz
- ✧ Small signal gain: 20dB
- ✧ Noise figure:1.8dB
- ✧ P1dB: 0dBm
- ✧ DC Supply: Vd=1.2V@Id=24mA (Vg=-0.41V)
- ✧ Dimensions: 1.7 mm×0.9 mm×0.07 mm

Product Description

GLA-4775 is an V-band broadband low noise amplifier chip with a frequency range of 47GHz~75GHz, small signal gain of 20dB and a typical noise figure of 1.8dB.

Die Outline Dimensions



Notes: 1) All dimensional units are micrometers (μm).

2) Tolerance for die length and width: ±50 μm.

3) Die thickness: 70 μm

Electrical Specifications

(Vd=1.2V，Id=24mA，TA=+25℃)

Parameter	Min	Typ	Max	Unit
Frequency range	47		75	GHz
Small signal gain		20		dB
Gain flatness		±1.0		dB
Noise figure		1.8		dB
P1dB		0		dBm
Input VSWR		1.5		-
Output VSWR		1.5		-
Quiescent Current		24		mA

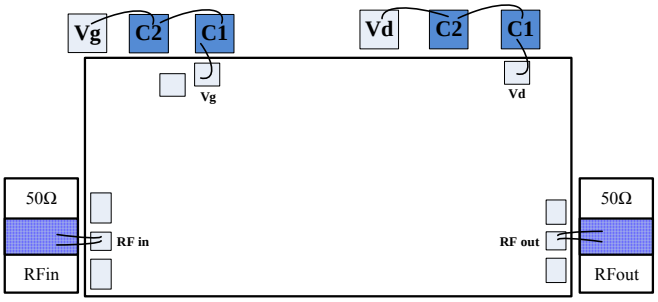
Absolute Maximum Ratings

Maximum Negative Gate Voltage	-1V
Maximum Drain Voltage	4V
Maximum Input RF Power	10dBm
Storage Temperature	-65℃~150℃
Operating Temperature	-55℃~85℃

Bond Pad Definition

No.	Symbol	Function Description	Pad Size(μm^2)
1	RFin	RF input port, matched to 50Ω system. No series DC blocking capacitor required	80×80
2	RFout	RF output port, matched to 50Ω system. No series DC blocking capacitor required	80×80
3	Vg	Gate bias supply pin; 100 pF and 10000 pF bypass capacitors shall be externally mounted.	100×100
4	Vd	Drain bias supply pin; 100 pF and 10000 pF bypass capacitors shall be externally mounted.	100×100

Recommended Assembly Schematic



Note: The peripheral capacitor C1 has a capacitance of 100 pF, and C2 is 10000 pF. Single-layer capacitor is recommended for C1, which shall be placed as close as possible to the chip bonding pads.It is recommended to add an external 10 μF bypass capacitor for both Vg and Vd.

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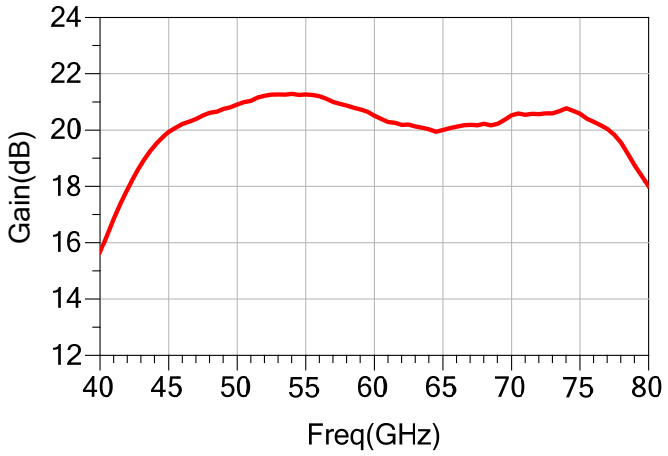
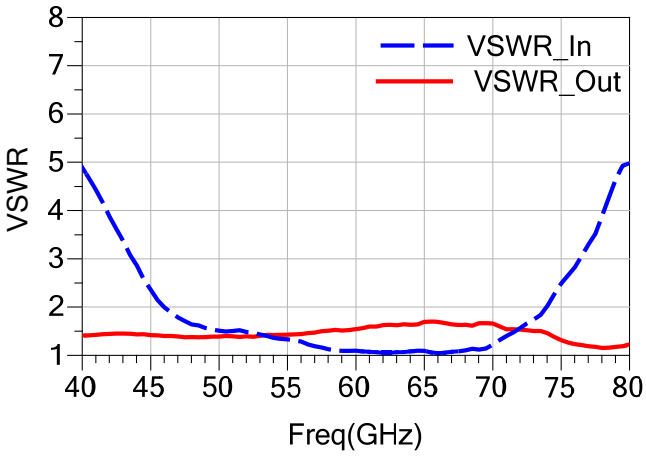
On-Wafer Measurement Curves Vd=1.2V，Id=24mA @ Vg=-0.41V

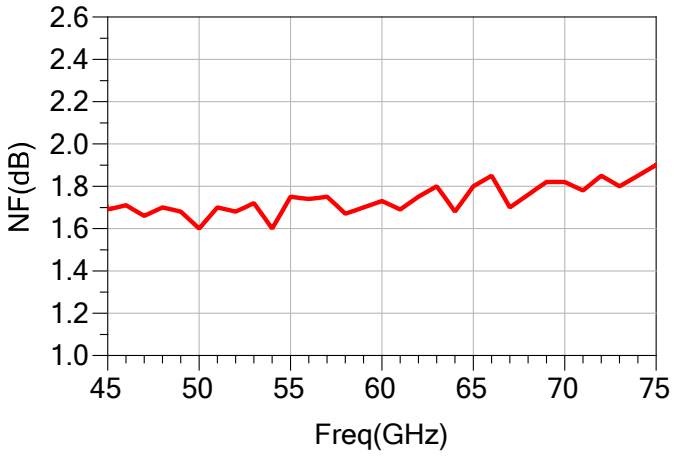
Small Signal Gain vs. Frequency



Input VSWR/Output VSWR vs. Frequency



Noise Figure vs. Frequency



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Handling & Operating Precautions

1) Storage: Dies must be stored in ESD-protected containers under nitrogen atmosphe

2) Cleaning: All die handling shall be performed in a cleanroom environment. Liquid cleaning solvents are prohibited for die cleaning. die handling shall be performed in a cleanroom environment. Liquid cleaning solvents are prohibited for die cleaning.

3) ESD Protection: Strictly follow all ESD control protocols to prevent electrostatic damage to the die.

4) General Handling: Handle dies only with vacuum pick-up tools or precision fine-tip tweezers. Avoid contact between tools/fingers and the die surface.

5) Power-up & Power-down Sequence: Power-up: Apply gate voltage first, then drain voltage.Power-down: Remove drain voltage first, then gate voltage.

6) Die Mounting: Two acceptable processes are AuSn eutectic sintering or conductive epoxy bonding. The mounting substrate surface must be clean and flat; minimize the gap between the die and RF input/output substrate traces.

- Sintering Process: Use 80/20 AuSn solder. Sinter temperature shall not exceed 300℃, total sinter time ≤20 seconds, scrub time ≤3 seconds.
- Epoxy Bonding: Apply minimal conductive epoxy dosage; follow curing specifications provided by epoxy supplier.

7) Wire Bonding Requirements:

- Unless otherwise specified, use two 25μm diameter gold bonding wires for RF input and output, with shortest possible wire length.
- Thermosonic bonding temperature: 150℃； use minimum feasible ultrasonic power.

8) Contact your supplier for technical support if any issues occur.