Standard Circuit

GLA-4053B

Low Noise Amplifier，40-53GHz

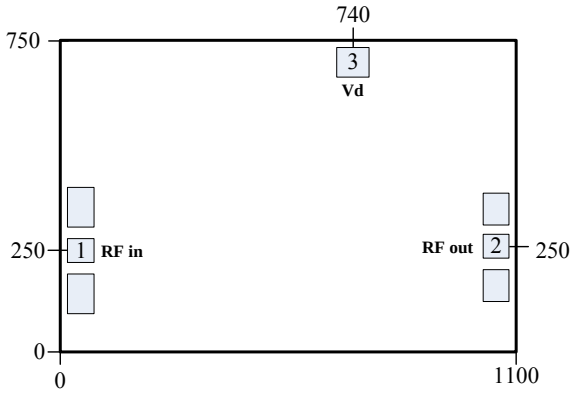
Performance characteristics

- ✧ Frequency range: 40GHz~53GHz
- ✧ Small signal gain: 21dB
- ✧ Noise figure:1.9dB
- ✧ P1dB: 4dBm
- ✧ DC Supply: Vd=5V@Id=13mA
- ✧ Dimensions: 1.10 mm×0.75 mm×0.07 mm

Product Description

GLA-4753 is an Q-band broadband low noise amplifier chip with a frequency range of 40GHz~53GHz, small signal gain of 21dB and a typical noise figure of 1.9dB. This chip operates from a single +5 V power supply.

Die Outline Dimensions



Notes: 1) All dimensional units are micrometers (μm).

2) Tolerance for die length and width: ±50 μm.

3) Die thickness: 70 μm

Electrical Specifications

(Vd=5V，I d=11mA，T A=+25℃)

Parameter	Min	Typ	Max	Unit
Frequency range	40		53	GHz
Small signal gain		21		dB
Gain flatness		±0.5		dB
Noise figure		1.9		dB
P1dB		4		dBm
Input VSWR		1.8		-
Output VSWR		1.8		-
Quiescent Current		13		mA

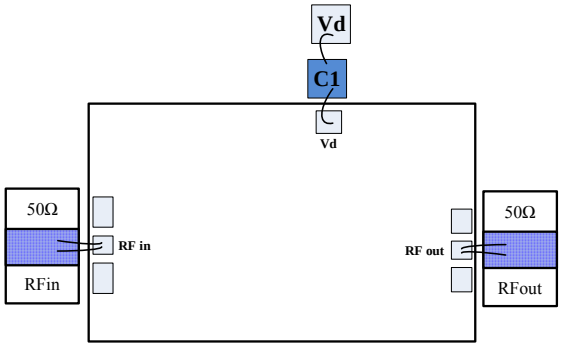
Absolute Maximum Ratings

Maximum Drain Voltage	8V
Maximum Input RF Power	15dBm
Storage Temperature	-65℃~150℃
Operating Temperature	-55℃~85℃

Bond Pad Definition

No.	Symbol	Function Description	Pad Size(μm^2)
1	RFin	RF input port, matched to 50Ω system. No series DC blocking capacitor required	80×80
2	RFout	RF output port, matched to 50Ω system. No series DC blocking capacitor required	80×80
3	Vd	Drain bias supply pin; 100 pF, a 100 pF bypass capacitor shall be externally fitted.	100×100

Recommended Assembly Schematic



Note: The peripheral capacitor C1 has a capacitance of 100 pF. A single-layer capacitor is recommended for C1 and should be placed as close as possible to the chip bonding pads.

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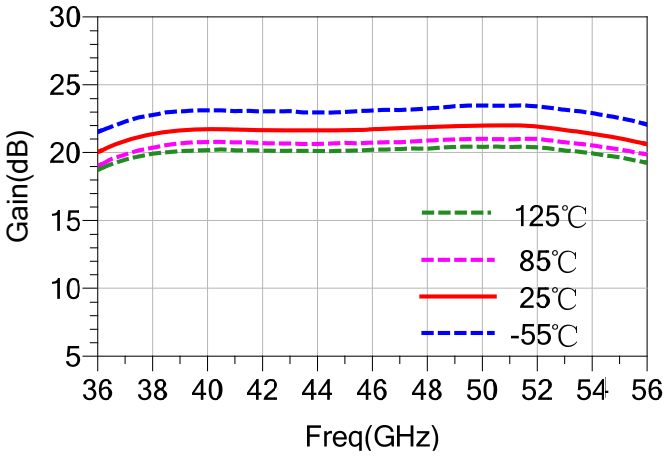
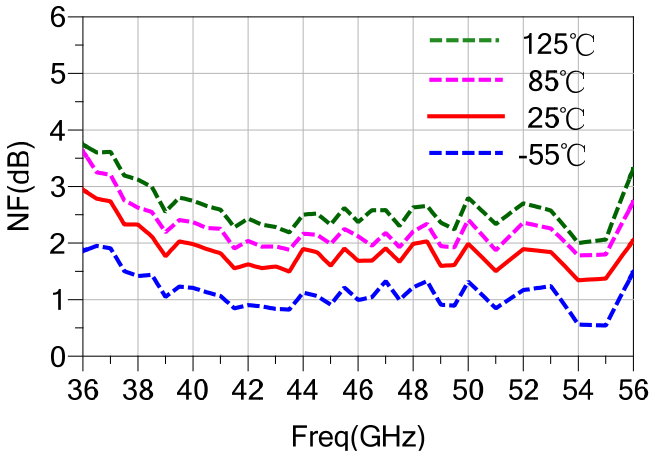
On-Wafer Measurement Curves Vd=5V，Id=13mA

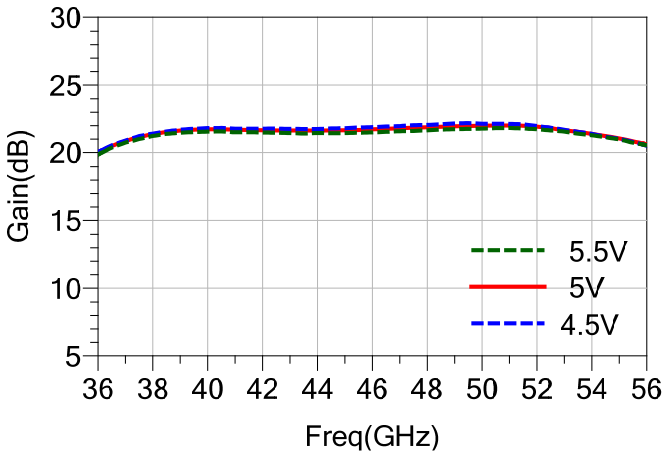
Small Signal Gain vs. Frequency



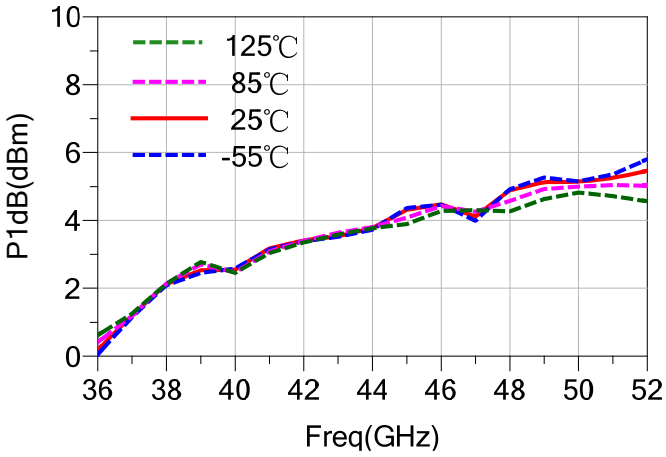
Noise Figure vs. Frequency



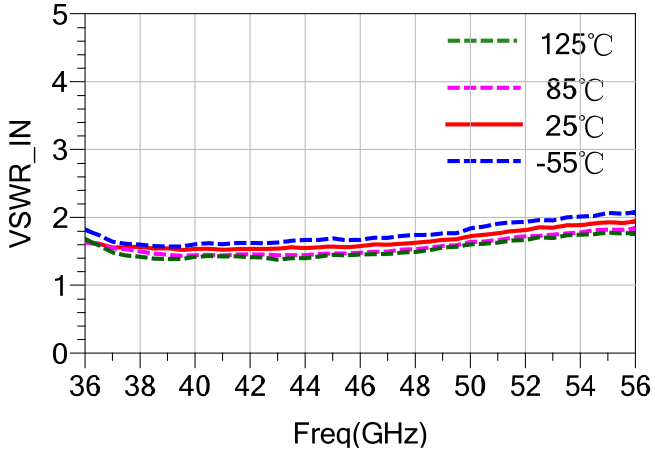
Small-signal gain vs. voltage



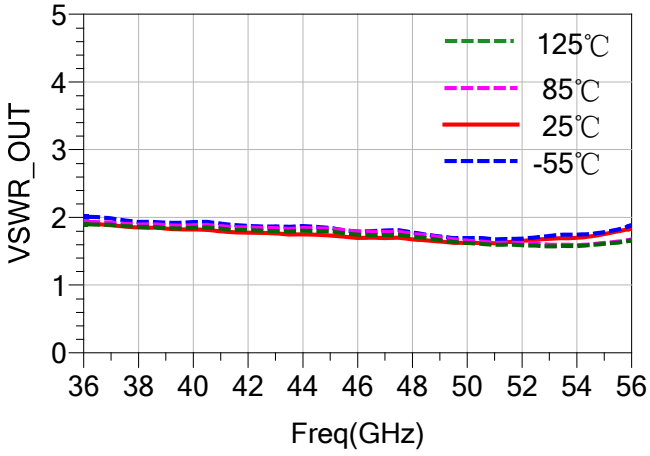
P1dB vs.Frequency



Input VSWR vs. Frequency



Output VSWR vs. Frequency



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Handling & Operating Precautions

1) Storage: Dies must be stored in ESD-protected containers under nitrogen atmosphe

2) Cleaning: All die handling shall be performed in a cleanroom environment. Liquid cleaning solvents are prohibited for die cleaning. die handling shall be performed in a cleanroom environment. Liquid cleaning solvents are prohibited for die cleaning.

3) ESD Protection: Strictly follow all ESD control protocols to prevent electrostatic damage to the die.

4) General Handling: Handle dies only with vacuum pick-up tools or precision fine-tip tweezers. Avoid contact between tools/fingers and the die surface.

5) Power-up & Power-down Sequence: Power-up: Apply gate voltage first, then drain voltage.Power-down: Remove drain voltage first, then gate voltage.

6) Die Mounting: Two acceptable processes are AuSn eutectic sintering or conductive epoxy bonding. The mounting substrate surface must be clean and flat; minimize the gap between the die and RF input/output substrate traces.

- Sintering Process: Use 80/20 AuSn solder. Sinter temperature shall not exceed 300℃, total sinter time ≤20 seconds, scrub time ≤3 seconds.
- Epoxy Bonding: Apply minimal conductive epoxy dosage; follow curing specifications provided by epoxy supplier.

7) Wire Bonding Requirements:

- Unless otherwise specified, use two 25μm diameter gold bonding wires for RF input and output, with shortest possible wire length.
- Thermosonic bonding temperature: 150℃； use minimum feasible ultrasonic power.

8) Contact your supplier for technical support if any issues occur.