

Performance characteristics

- ✧ Frequency range: 37GHz~43GHz
- ✧ Small signal gain: 24dB
- ✧ Noise figure: 2.2dB
- ✧ P1dB: 4dBm
- ✧ DC Supply: $V_d=5V@I_d=11mA$
- ✧ Dimensions: 1.30 mm×0.65 mm×0.07 mm

Product Description

GLA-3743 is an Q-band broadband low noise amplifier chip with a frequency range of 37GHz~43GHz, small signal gain of 24dB and a typical noise figure of 2.2dB.

Electrical Specifications

($V_d=5V$, $I_d=11mA$, $T_A=+25^{\circ}C$)

Parameter	Min	Typ	Max	Unit
Frequency range	37		43	GHz
Small signal gain		24		dB
Gain flatness		± 0.25		dB
Noise figure		2.2		dB
P1dB		4		dBm
Input VSWR		1.6		-
Output VSWR		2.0		-

Absolute Maximum Ratings

Maximum Drain Voltage	8V
Maximum Input RF Power	15dBm
Storage Temperature	$-65^{\circ}C \sim 150^{\circ}C$
Operating Temperature	$-55^{\circ}C \sim 85^{\circ}C$

Low Noise Amplifier, 37-43GHz

Die Outline Dimensions

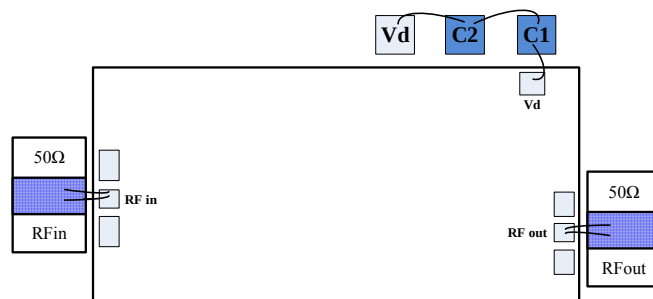


- Notes: 1) All dimensional units are micrometers (μm).
 2) Tolerance for die length and width: $\pm 50 \mu m$.
 3) Die thickness: 70 μm

Bond Pad Definition

No.	Symbol	Function Description	Pad Size(μm^2)
1	RFin	RF input port, matched to 50 Ω system. No series DC blocking capacitor required	80×80
2	RFout	RF output port, matched to 50 Ω system. No series DC blocking capacitor required	80×80
3	Vd	Drain bias supply pin; 100 pF, 1000 pF shunt bypass capacitors are required externally.	100×100

Recommended Assembly Schematic

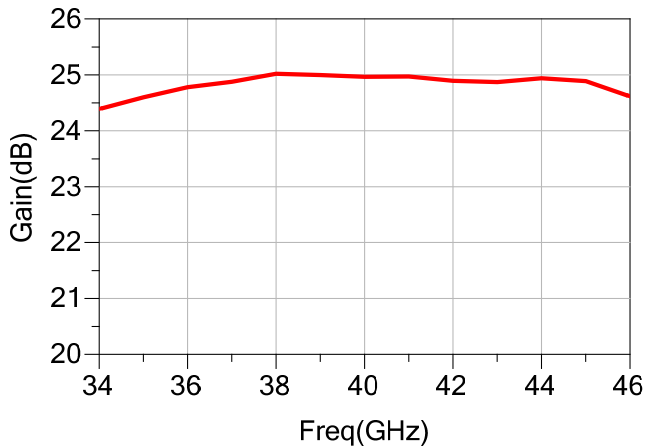


Note: The peripheral capacitor C1 is 100 pF and C2 is 10000 pF. It is recommended to use a single-layer capacitor for C1 and place it as close as possible to the chip bonding pads.

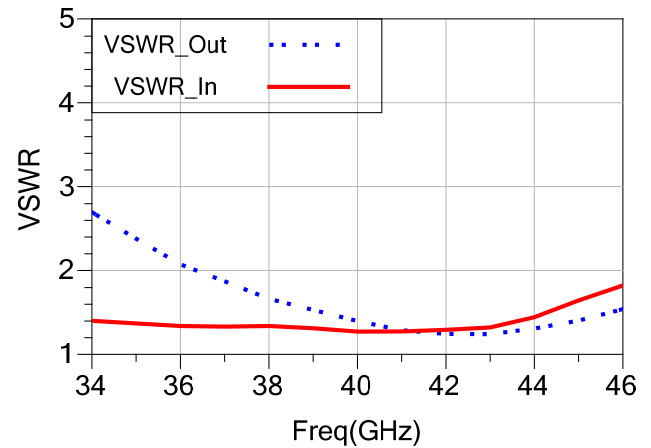
Low Noise Amplifier, 37-43GHz

On-Wafer Measurement Curves($T_A=+25^{\circ}\text{C}$) $V_d=5\text{V}$, $I_d=11\text{mA}$

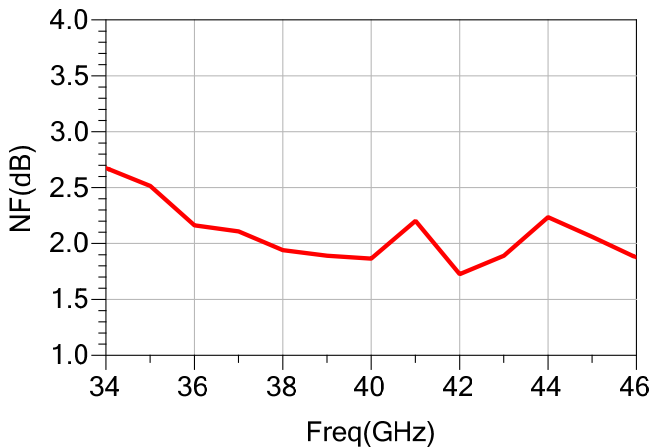
Small Signal Gain vs. Frequency



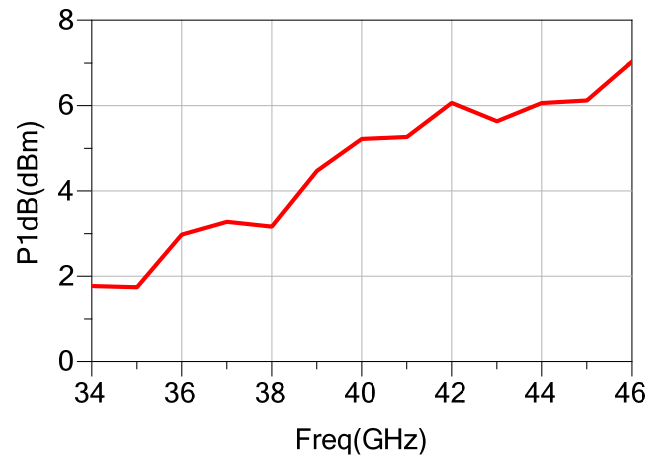
Input VSWR/Output VSWR vs. Frequency



Noise Figure vs. Frequency



P1dB vs. Frequency



Low Noise Amplifier, 37-43GHz

Handling & Operating Precautions

- 1) Storage: Dies must be stored in ESD-protected containers under nitrogen atmosphere.
- 2) Cleaning: All die handling shall be performed in a cleanroom environment. Liquid cleaning solvents are prohibited for die cleaning. die handling shall be performed in a cleanroom environment. Liquid cleaning solvents are prohibited for die cleaning.
- 3) ESD Protection: Strictly follow all ESD control protocols to prevent electrostatic damage to the die.
- 4) General Handling: Handle dies only with vacuum pick-up tools or precision fine-tip tweezers. Avoid contact between tools/fingers and the die surface.
- 5) Power-up & Power-down Sequence: Power-up: Apply gate voltage first, then drain voltage. Power-down: Remove drain voltage first, then gate voltage.
- 6) Die Mounting: Two acceptable processes are AuSn eutectic sintering or conductive epoxy bonding. The mounting substrate surface must be clean and flat; minimize the gap between the die and RF input/output substrate traces.
 - Sintering Process: Use 80/20 AuSn solder. Sinter temperature shall not exceed 300 °C, total sinter time ≤20 seconds, scrub time ≤3 seconds.
 - Epoxy Bonding: Apply minimal conductive epoxy dosage; follow curing specifications provided by epoxy supplier.
- 7) Wire Bonding Requirements:
 - Unless otherwise specified, use two 25µm diameter gold bonding wires for RF input and output, with shortest possible wire length.
 - Thermosonic bonding temperature: 150 °C; use minimum feasible ultrasonic power.
- 8) Contact your supplier for technical support if any issues occur.