

Power amplifier, GPA-12.5-14.5-35.5

Parameters

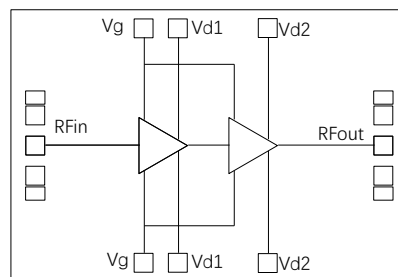
- Operating frequency: 12.5~14.5GHz
- Linear gain: 18.5dB
- Psat: 35.5dBm
- Power supply: 7V/1.1A
- 50ohm input/output
- Chip size: 2.20mm×2.40mm×0.1mm



Product introduction

GPA-12.5-15-35 is a power amplifier chip manufactured using GaAs pHEMT technology. The working frequency band covers max 12.5-15GHz. Under a bias voltage of 7V, the linear gain of the chip is 18.5dB, the output P-1dB power is 34.5dBm, the saturated output power is 35dBm, and the power added efficiency is 40%. The chip is grounded through the back through-hole and powered by dual power sources, mainly used in communication systems, transceiver components, and other fields.

Bare die block diagram



Max. operating conditions^[1]

Parameter	Ratings
Drain voltage	+10V
Input power	+20dBm
Operating temperature	-55°C~+85°C
Storage temperature	-65°C~+120°C

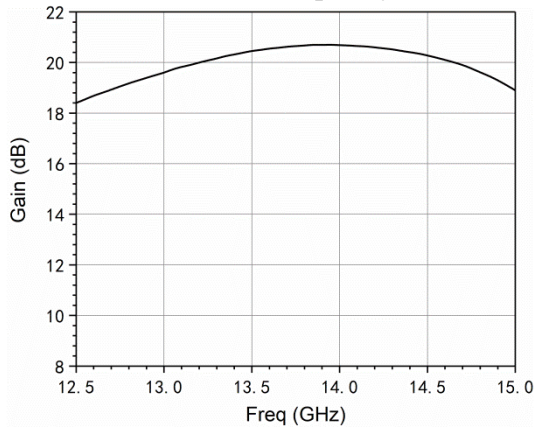
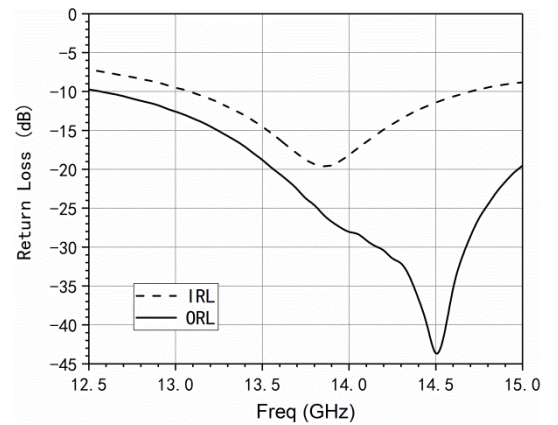
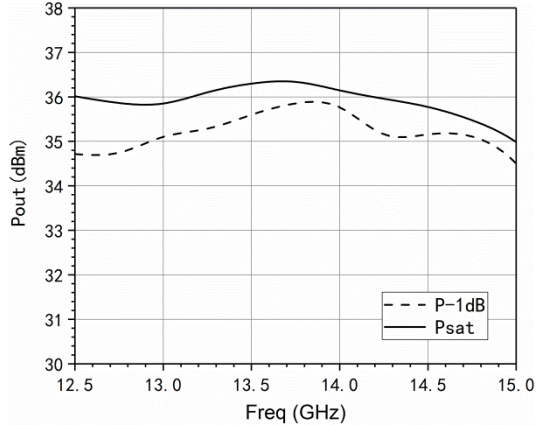
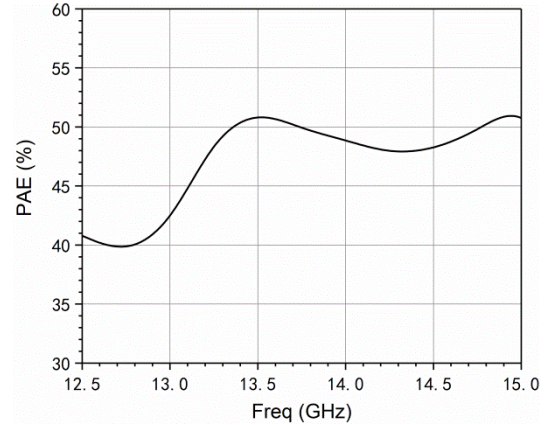
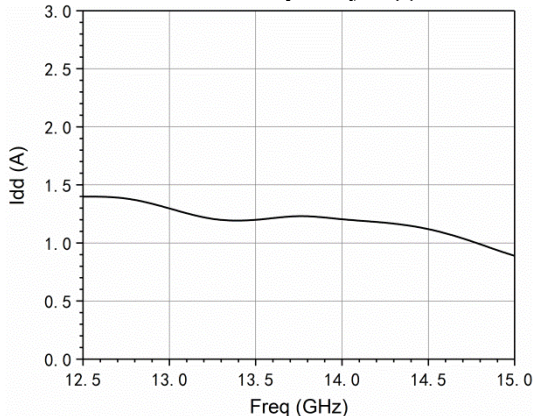
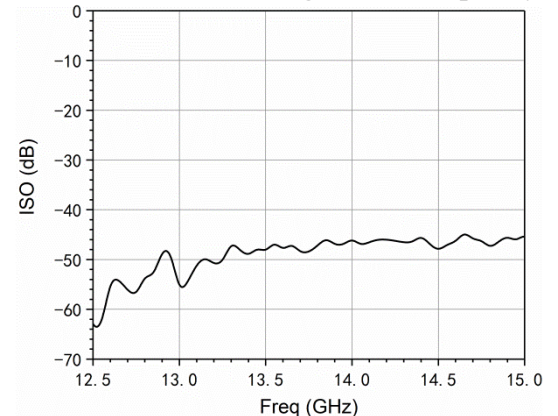
[1] Exceeding any of these limits may cause permanent damage.

DC electrical specifications (TA=+25 °C, Vd=+7V)

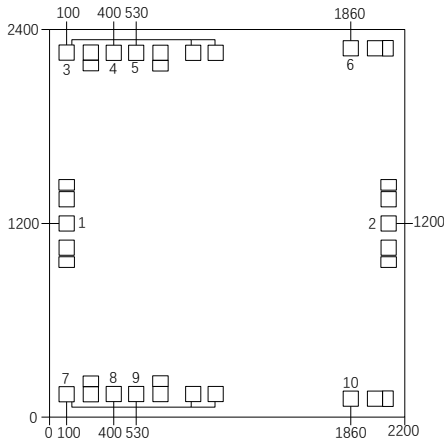
Parameter	Min	Typ	Max	Unit
Drain working voltage		7	8	V
Gate bias voltage	-0.8	-0.7	-0.6	V
Quiescent drain current		1.1		A

Microwave electrical specifications (TA=+25 °C, Vd=+7V)

Parameter	Min	Typ	Max	Unit
Frequency range	12.5~14.5			GHz
Linear gain	18.4	20	20.8	dB
Gain flatness		±1.2		dB
P-1dB	34.5	35.5		dBm
Psat	35	35.5		dBm
PAE	40			%
Input return loss		-15	-7	dB
Output return loss		-20	-10	dB

Typical test results (Vd: +7V)
Gain VS. Frequency

Input/output return loss VS. Frequency

P1dB&Psat VS. Frequency

PAE VS. Frequency

Idd VS. Frequency (@Psat)

Reverse isolation degree VS. Frequency


Outline dimensions



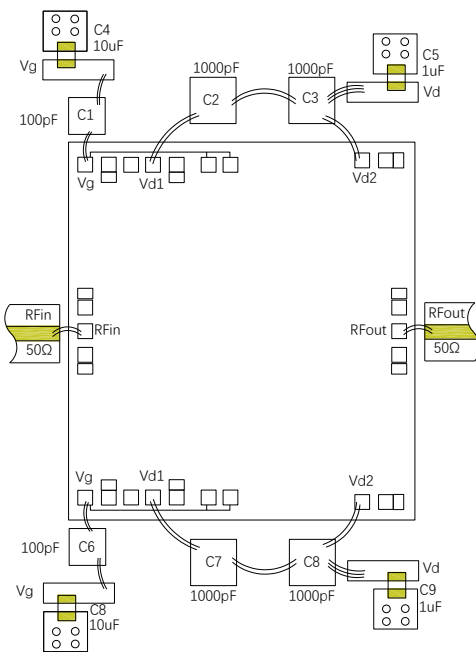
Notes:

1. Unit: μm
2. Gold plating on bonding pads
3. Dimensional tolerance: $\pm 20\mu\text{m}$

Pad Definition

Pad Number	Function	Description	Dimensions
1	IN	RF input, external 50 ohm system, no need for external blocking capacitor	100×100 μm
2	OUT	RF output, external 50 ohm system, no need for external blocking capacitor	100×100 μm
3、7	VG	Gate power supply, requiring an external 100pF filtering capacitor	100×100 μm
4、8	VD1_Test	Drain 1 power supply, not connected when not being testing	100×100 μm
5、9	VD1	Drain 1 power supply, requiring an external 1000pF single-layer chip capacitor	100×100 μm
6、10	VD2	Drain 2 power supply, requiring an external 1000pF single-layer chip capacitor	100×100 μm

Suggested assembly diagram

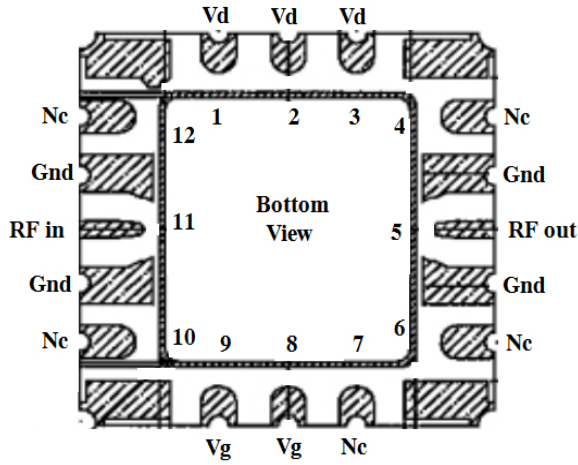


Note:

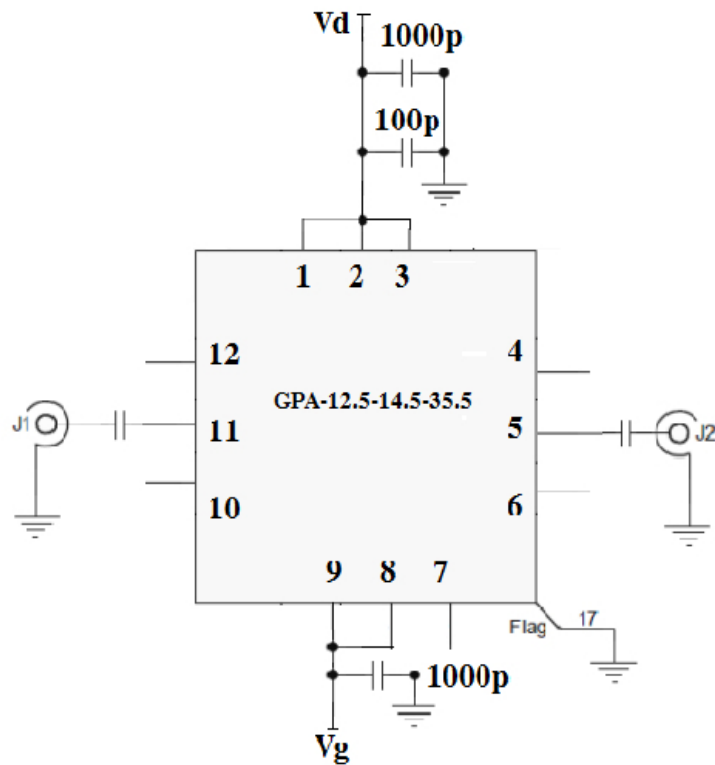
1. Please assemble and use in a purified environment, store in anti-static containers, and keep dry
2. The back of the chip is grounded with gold backing. Please ensure that the back is in full contact with the ground and well grounded during use
3. When using conductive silver adhesive for chip bonding, do not use too much conductive silver adhesive and do not touch the upper surface of the chip
4. Use gold tin solder with a ratio of 80/20 to sinter, with a sintering temperature not exceeding 300 °C and a sintering time as short as possible, not exceeding 20 seconds
5. This product is an electrostatic sensitive device. Please pay attention to anti-static measures during storage and use
6. Do not attempt to clean the surface of the chip using dry or wet chemical methods
7. If you have any questions, please contact the supplier

Note: To ensure more stable performance of the amplifier, it is recommended to weld ceramic capacitors with the recommended capacitance values in the above assembly diagram at the feeding end for filtering. The number of filtering capacitors can also be increased or different capacitance values can be combined according to actual needs.

QFN Bottom view diagram



Application schematic diagram



Note: To ensure more stable performance of the amplifier, it is recommended to weld ceramic capacitors with the recommended capacitance values in the above assembly diagram at the feeding end for filtering. The number of filtering capacitors can also be increased or different capacitance values can be combined according to actual needs.