Standard Circuit

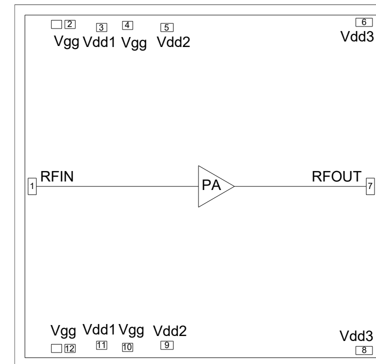
GPA15-18-44

GaN MMIC Power Amplifier Chip, 15-18 GHz

Performance characteristics

- Frequency range: 15.0~18.0GHz
- Psat: 44.5dBm@Pin=21dBm
- Power gain: 23.5dB@Pin=21dBm
- PAE: 35%@Pin=21dBm
- Power supply: 28V/1.8A
- 50ohm input/output
- Chip size: 3.6mm×3.5mm×0.08mm

Block Diagram



Product Introduction

GPA15-18-44 is a GaN monolithic integrated power amplifier chip operating at 15.0-18.0GHz. At a pulse width of 100us, a duty cycle of 10%, and a working voltage of+28V, a power gain of 22.5dB can be provided, with a saturated output power of 44.5dBm and a power added efficiency of 35%. The chip is grounded through the vias. Mainly used in communication systems, high-power transceiver components, and other fields.

DC electrical specifications (TA=+25 ℃)

Parameter	Min	Typ	Max	Unit
Gate bias voltage		-1.9		V
Drain working voltage		28		V
Quiescent drain current		1.8		A
Dynamic drain current		3.5		A

Note: Adjust the gate voltage Vgg between -3.0V and -1.5V to achieve a quiescent current Idq=800mA

Microwave electrical parameters (TA=+25℃, Vd=+28V, pulse width 100us, duty cycle 10%)

Parameter	Min	Typ	Max	Unit
Frequency range	15.0~18.0			GHz
Small signal gain		34		dB
Psat		44.5		dBm
PAE	35			%
Power gain(Pin=21dBm)		23.5		dB
Input return loss		-15	-8	dB

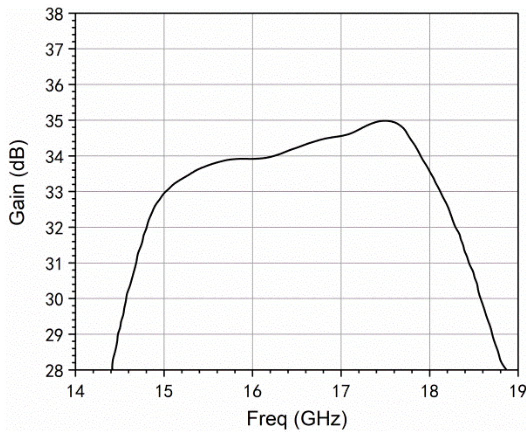
Absolute maximum ratings[1]

Parameter	Ratings
Drain voltage	+35V
Gate voltage	-6~-1V
Operating temperature	-55℃~+85℃
Storage temperature	-55℃~+150℃

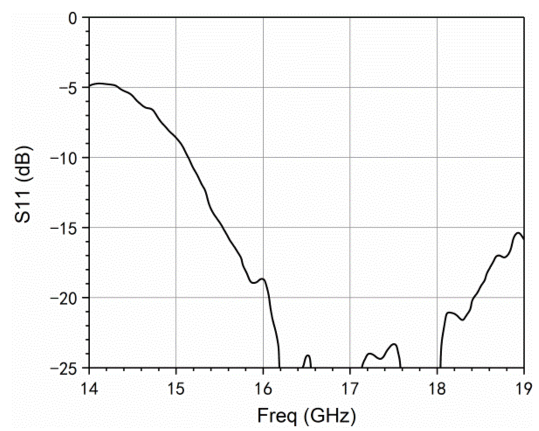
[1] Exceeding any of these limits may cause permanent damage.

Typical performance curves (Vd:+28V, quiescent Id=1.8A, pulse width 100us, duty cycle 10%)

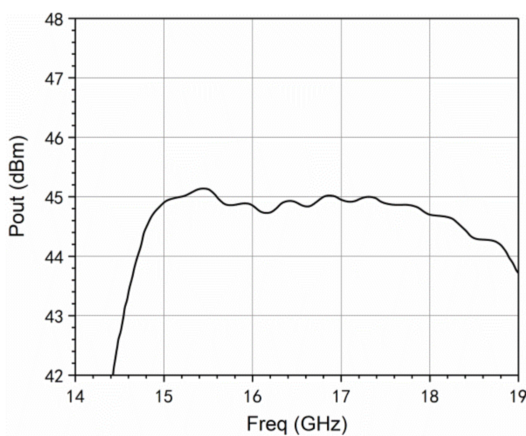
Small signal gain VS. Frequency



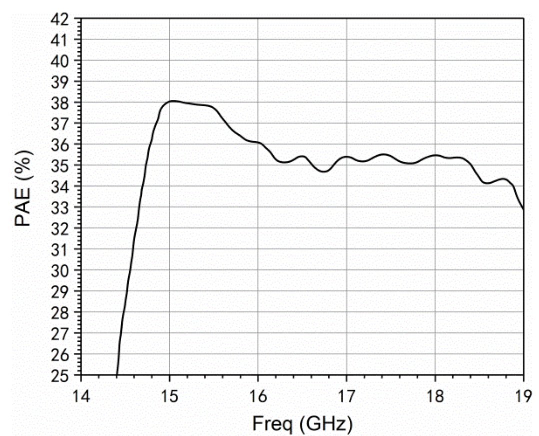
Input return loss VS. Frequency



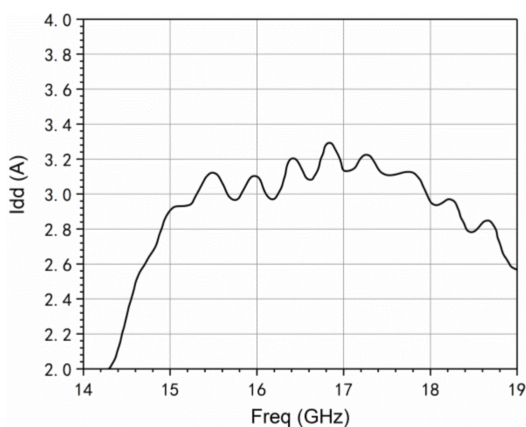
Psat VS. Frequency (Pin=21dBm)



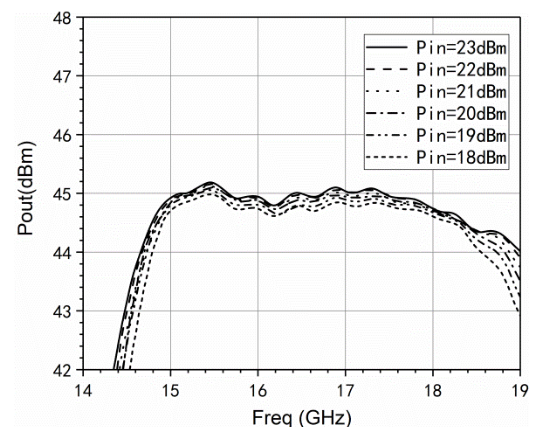
PAE VS. Frequency



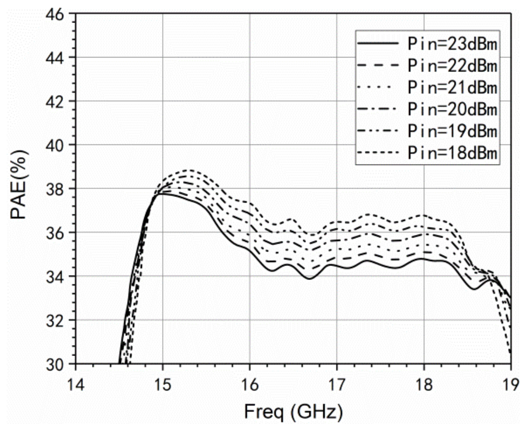
Drain current VS. Frequency (Pin=21dBm)



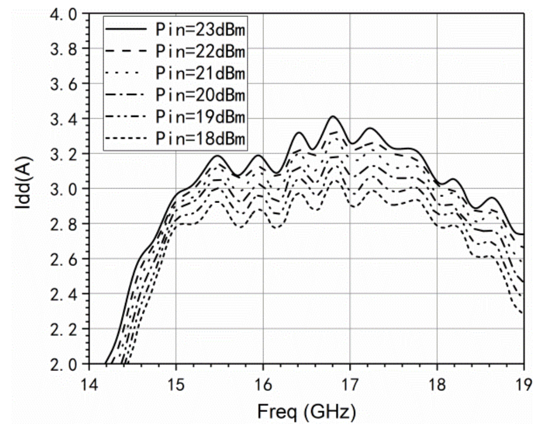
Output power VS. Frequency VS. Input power



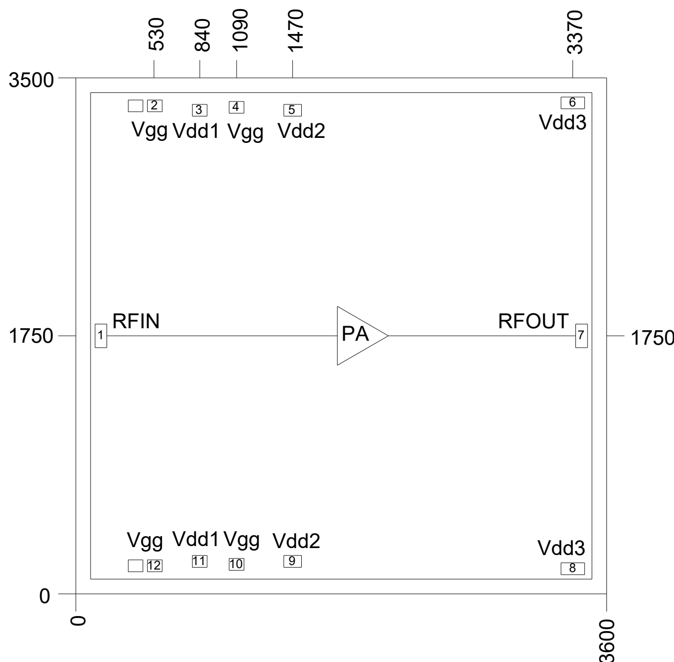
PAE VS. Frequency VS. Input power



Drain current VS. Frequency VS. Input power



Outline dimensions



Notes:

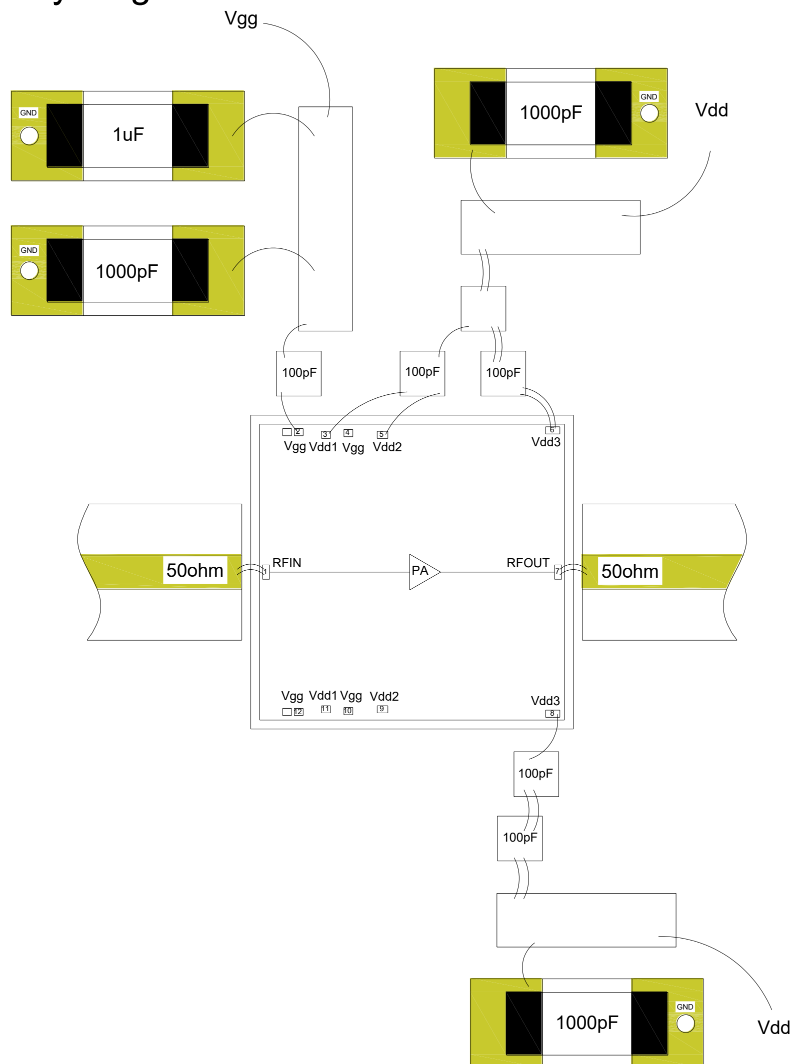
1. Unit: μm
2. Gold plating on bonding pads
3. Dimensional tolerance: ± 20μm
4. Bonding pad size:

   1、6、7、8：100×200um
   2、3、4、10、11、12：
   100×100um 5、9：100×150um

Pad Definition

Pad Number	Function	Description
1	RFIN	RF input, external 50 ohm system
2、4、10、12	Vgg	Amplifier gate bias voltage point, typical voltage is -1.9V
3、11	Vdd1	Amplifier drain bias voltage, requiring an external 100pF bypass capacitor
5、9	Vdd2	Transmitting amplifier drain bias voltage, requiring external 100pF bypass capacitor
6、8	Vdd3	Receiving amplifier drain bias voltage, requiring external 100pF bypass capacitor
7	RFOUT	RF output, external 50 ohm system

Suggested assembly diagram



Note: The filtering capacitor should be as close as possible to the chip voltage point to minimize the impact of bonding wire length.

Note:

1. Please assemble and use in a purified environment, store in anti-static containers, and keep dry
2. The back of the chip is grounded with gold backing. Please ensure that the back is in full contact with the ground and well grounded during use
3. Use gold tin solder with a ratio of 80/20 to sinter, with a sintering temperature not exceeding 300 °C and a sintering time as short as possible, not exceeding 20 seconds
4. This product is an electrostatic sensitive device. Please pay attention to anti-static measures during storage and use
5. Do not attempt to clean the surface of the chip using dry or wet chemical methods
6. If you have any questions, please contact the supplier

This product is sensitive to static electricity. Please pay attention to anti-static measures during use

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