

GaN MMIC Power Amplifier Chip, 14-18 GHz

Performance characteristics

• Frequency range: 14.0~18.0GHz Block Diagram

Saturated output power: 42dBm

PAE: 36%

Power gain: 20dB

Power supply: +28V/-1.9V

• Chip size: 3.0mmx2.0mmx0.08mm

Product Introduction

GPA14-18-42 is a GaN monolithic integrated power amplifier chip that operates between 14.0-18.0GHz. With a pulse width of 100us, a duty cycle of 10%, and a working voltage of+28V, it can provide 20dB power gain and 42dBm saturated output power, with a power added efficiency of 36%. The power amplifier chip adopts on-chip via metallization technology to ensure good grounding, without the need for additional grounding measures, making it simple and convenient to use. The back of the chip has been metalized and is suitable for eutectic sintering process.

DC electrical specifications (TA=+25 °C)

Parameter	Min	Тур	Max	Unit
Gate bias voltage		-1.9		V
Drain working voltage		28		V
Quiescent drain current		700		mA
Dynamic drain current			1800	mA

Microwave electrical parameters (TA=+25℃, Vd=+28V, pulse width 100us, duty cycle 10%)

Parameter	Min	Тур	Max	Unit
Frequency range	14.0~18.0		GHz	
Small signal gain		28		dB
Psat		42		dBm
PAE		36		%
Power gain		20		dB
Input return loss		10		dB

Absolute maximum ratings[1]

Parameter	Ratings	
Input power, pulse 50 Ω	+28dBm	
Drain voltage	+33V	
Gate voltage	-6V~-1V	
TCH	225℃	
Sintering temp., 20s, N2 protection	300℃	
Operating temperature	-55℃~+150℃	
Storage temperature	-55℃~+85℃	

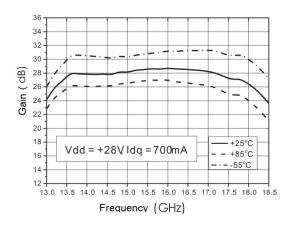
[1] Exceeding any of these limits may cause permanent damage.



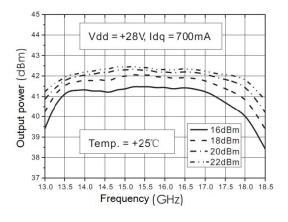
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Typical performance curves (Vd:+28V, quiescent ld=1700mA, pulse width 100us, duty cycle 10%)

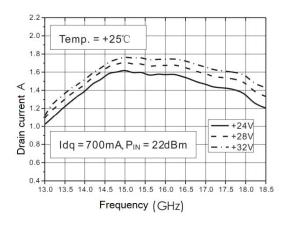
Small signal gain VS. Frequency VS. Temp.



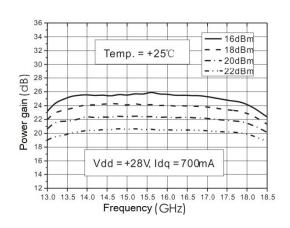
Output power VS. Frequency



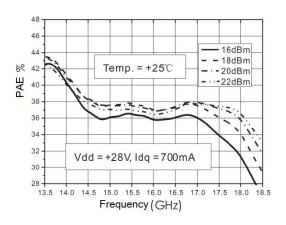
Dynamic current VS. Frequency



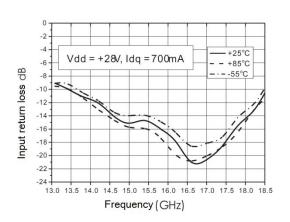
Power gain VS. Frequency



PAE VS. Frequency



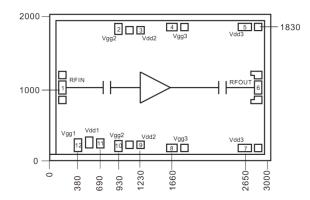
Input return loss VS. Frequency





Outline dimensions

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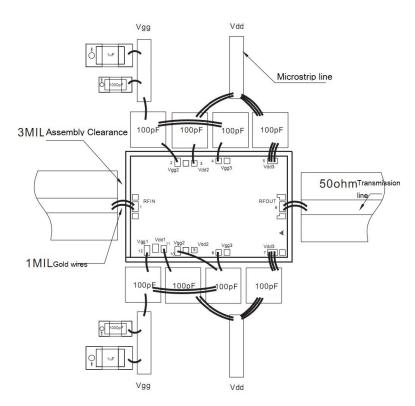
Notes:

- 1. Unit: um
- 2. Gold plating on bonding pads
- 3. Dimensional tolerance: ± 20µm

Pad Definition

Pad Number	Function	Description
1	IN	RF input, external 50 ohm system, no need for external blocking capacitor
2、4、8、10、12	Vg	Amplifier gate bias voltage, requiring external 100pF, 1000pF, and 1uF bypass capacitor
3、5、7、9、11	Vd	Amplifier drain bias voltage, requiring an external 100pF bypass capacitor
6	OUT	RF output, external 50 ohm system, no need for external blocking capacitor
Chip bottom	GND	The bottom of the chip needs to have good contact with RF and DC ground

Suggested assembly diagram



Note: To ensure more stable performance of the amplifier, it is recommended to weld ceramic capacitors with the recommended capacitance values in the above assembly diagram at the feeding end for filtering. Alternatively, the number of filtering capacitors can be increased or capacitors with different capacitance values can be used in combination according to actual needs. The filtering capacitor should be as close as possible to the chip voltage point to minimize the impact of bonding wire length.

Note:

- 1. Please assemble and use in a purified environment, store in anti-static containers, and keep dry.
- 2. The back of the chip is grounded with gold backing. Please ensure that the back is in full contact with the ground and well grounded during use.
- 3. Use gold tin solder with a ratio of 80/20 to sinter, with a sintering temperature not exceeding 300 °C and a sintering time as short as possible, not exceeding 20 seconds.
- 4. This product is an electrostatic sensitive device. Please pay attention to anti-static measures during storage and use.
- 5. Do not attempt to clean the surface of the chip using dry or wet chemical methods.
- 6. If you have any questions, please contact the supplier.