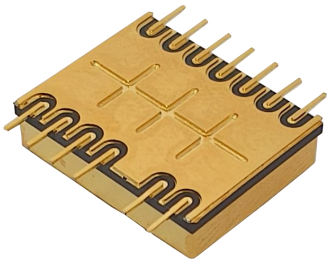
GF034-001T068A

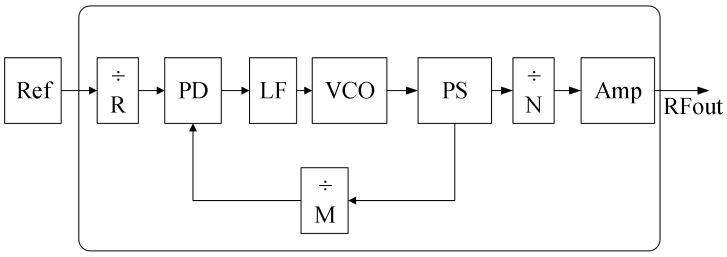
Mini universal frequency source D, 0.1～0.68GHz

Performance characteristics

- Operating frequency: 0.1～6.8GHz
- Frequency step: 1kHz～100MHz
- Output power: ≥0dBm
- Supply voltage: +3.3V
- Control mode: SPI
- Outline Dimensions: 15x12x3.5mm
- Packaging form: ceramic packaging
- Working temperature: -40℃～+85℃



Principle diagram



Product Introduction

GF034-001T068A is a mini universal frequency source with an output frequency range of 0.1-6.8GHz. It can achieve a minimum frequency hopping step of 1kHz and a typical phase noise value of -101dBc/Hz@1k@6GHz, -108dBc/Hz@10k@6GHz, output power ≥0dBm. It is housed in a ceramic package, suitable for SMT.

Electrical parameters(TA = +25°C, 50Ω system)				
Parameter	Min	Typ	Max	Unit
Operating frequency	0.1	4	6.8	GHz
Output power		⩾0		dBm
Frequency step	0.001	1	100	MHz
Spurious		⩾50		dBc
Phase noise		-104		dBc/Hz@1K
		-111		dBc/Hz@10K
		-120		dBc/Hz@100K
		-123		dBc/Hz@1M
Current		⩽260		mA

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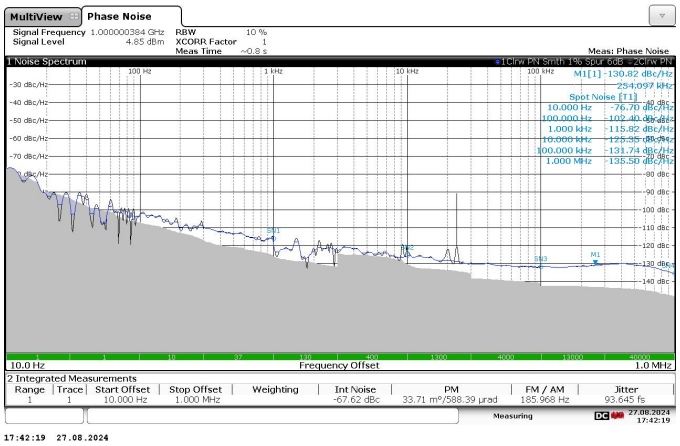
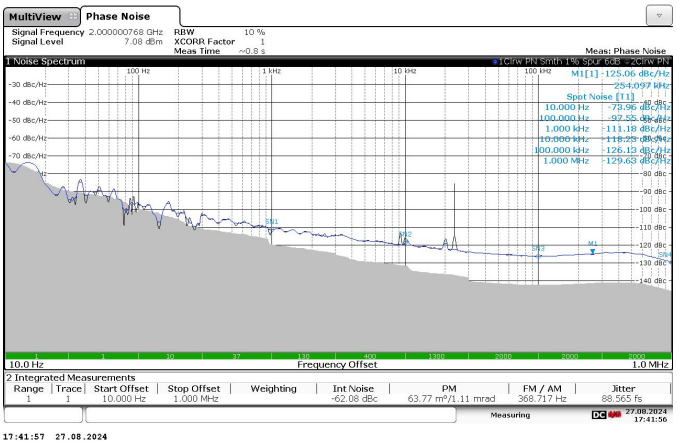
Main indicator testing curve

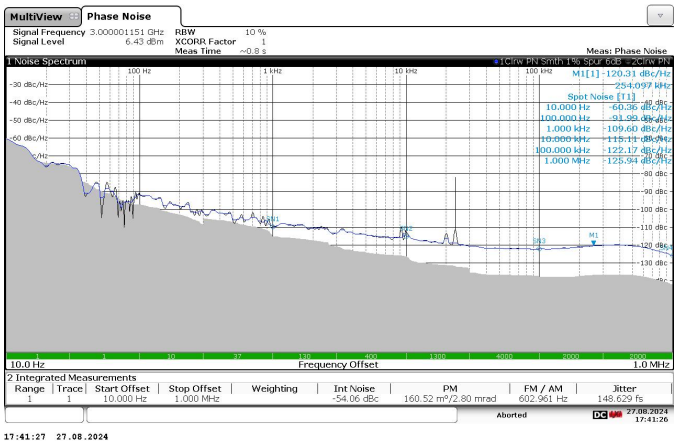
1GHz phase noise @25℃



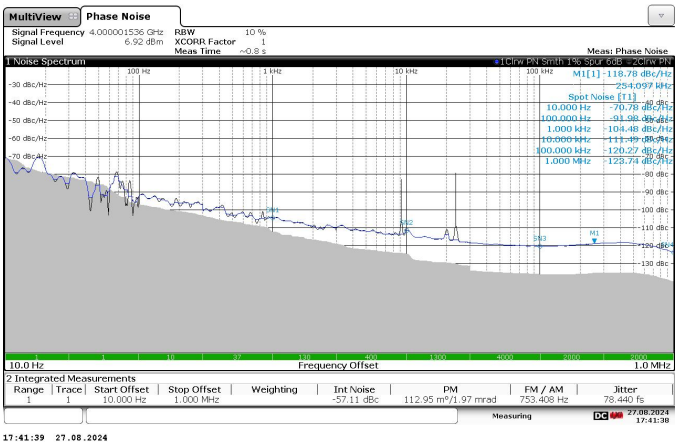
2GHz phase noise @25℃



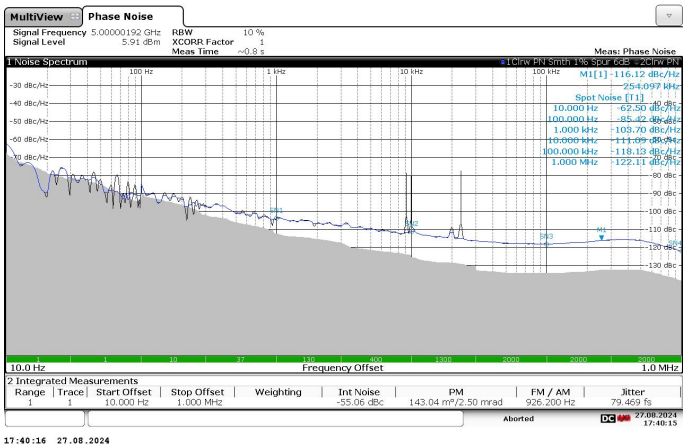
3GHz phase noise @25℃



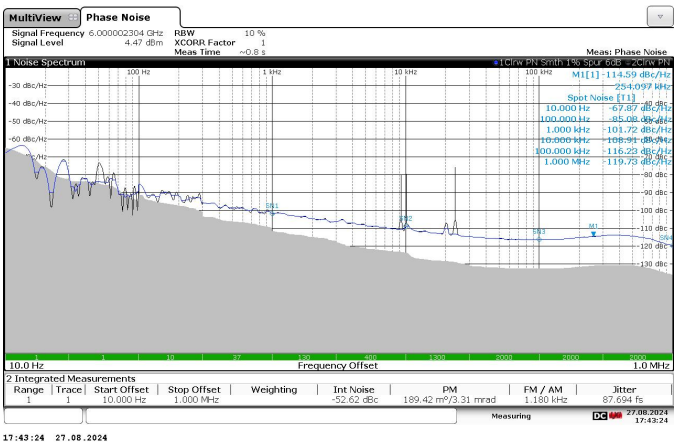
4GHz phase noise @25℃



5GHz phase noise @25℃



6GHz phase noise @25℃



2.0001GHz spurious @25℃

5.3011GHz spurious @25℃

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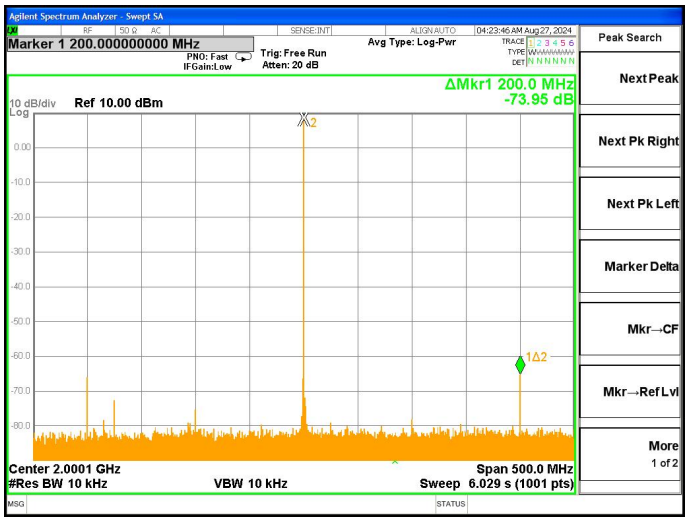
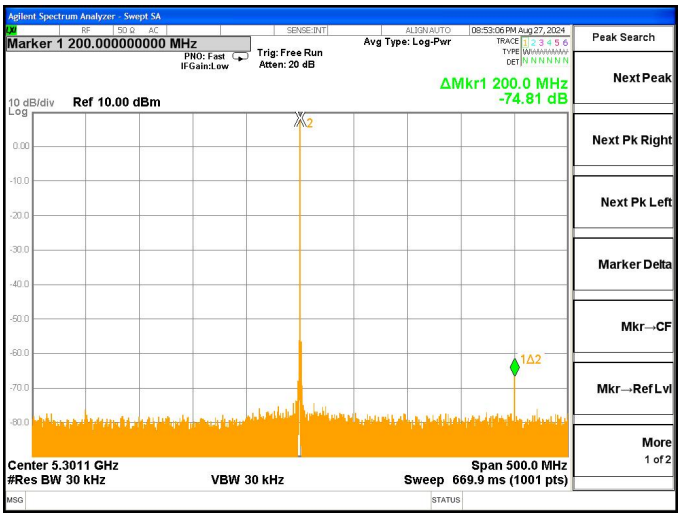
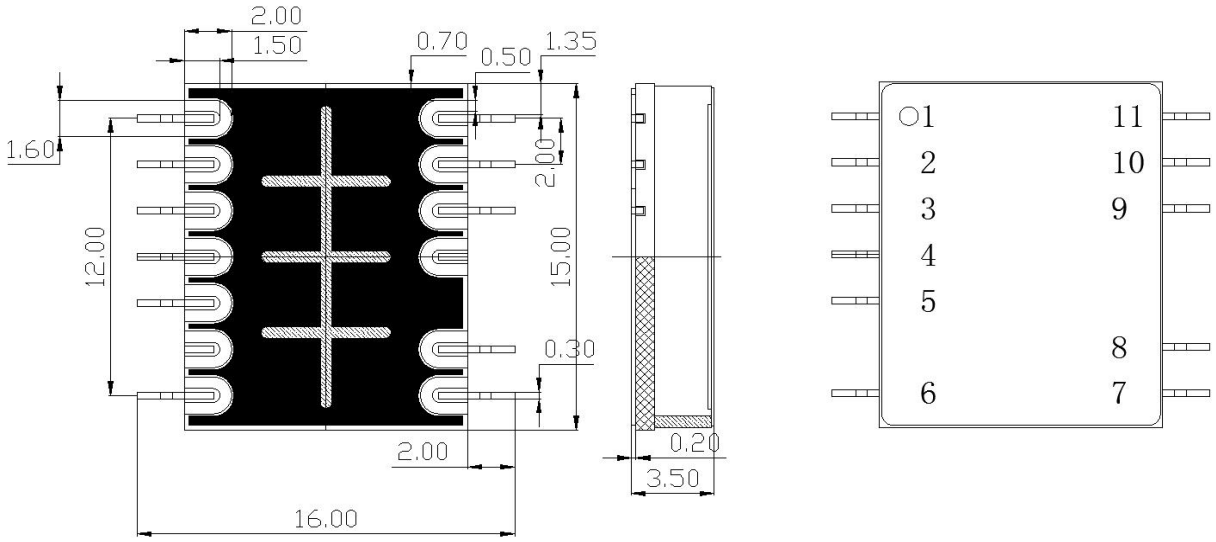




External structure



Pin	Function	Description
1	LE	Enable
2	DATA	data
3	CLK	Clock
4	LD	Lock indication: Locked at high level, unlocked at low level
5	REF	100M reference input
6	GND	Ground
7	+3.3V	+3.3V power supply
8	RFout	RF output
9	GND	Ground
10	NC	Not connected
11	NC	Not connected

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Control requirements

The output module frequency is controlled through SPI serial port, and the control method is as follows:

The total length of SPI serial port data DI is 64 bits (8 bytes), as shown in the table.

Definition of DI for receiving data								
—	D7	D6	D5	D4	D3	D2	D1	D0
The 1st byte	LSB							
. . .	. . .							
The 4th byte	MSB							

Remark：

- The order of receiving data is: first receive the first byte, then the second byte, until the 8th byte. In each byte, the high bits come first and the low bits come last;
- The frequency step is 1kHz.

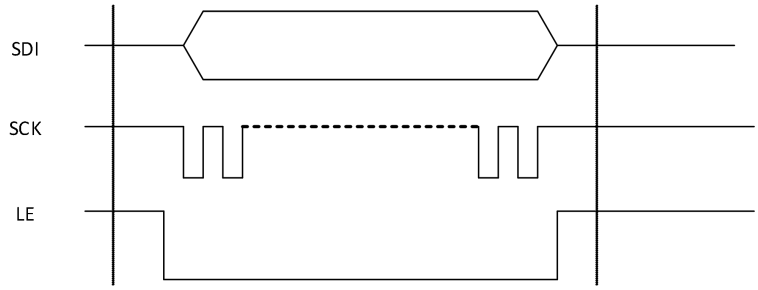

Fig. SPI serial port timing diagram

Instructions:

1) LE is the enable signal, when LE is at a low level, the data and clock signals are valid.

2) SCK is a clock signal that can support a maximum clock frequency of 10MHz， LVTTL level.

3) SDI is serial input data, valid when SCK rises, LVTTL level.

Remark

- Unit: mm;
- Frequency hopping time does not include communication time;
- The larger the step, the faster the hopping time, and the better the spurious;
- The power supply of the product needs to be filtered to prevent interference from power ripple on sensitive components;
- The device should be stored in a dry and nitrogen environment. When the device cannot be used up after being unpacked, it should be immediately stored in a drying oven or vacuum sealed to avoid

absorbing moisture from the air;

- Devices are sensitive to static electricity, and attention should be paid to anti-static measures during storage, transportation, assembly, and use;
- This product is suitable for reflow soldering installation process, with a maximum reflow soldering peak temperature of 210 ℃.