Standard Circuit

GLA-4053
Low Noise Amplifier Chip

Performance Characteristics

- Frequency range: 40GHz-53GHz
- Small signal gain: 21dB
- Noise figure: 1.9dB
- P1dB: 4dBm
- DC power supply: Vd= 5V@Id =13mA
- Chip size: 1.10 mm x 0.75 mm x 0.07 mm

Product Introduction

The Q-band low-noise amplifier chip has a frequency range of 40GHz to 53GHz, with a typical small signal gain of 21dB and a typical noise figure of 19dB. The chip is powered by a single 5V power supply.

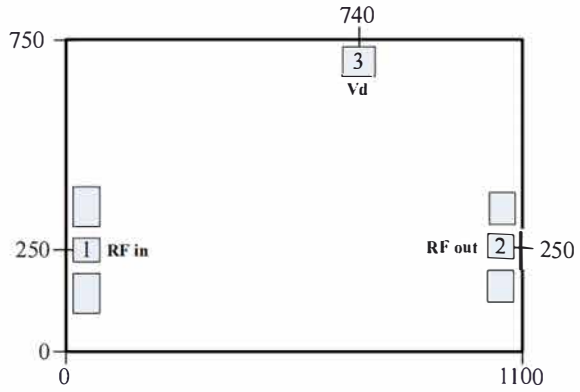
Electrical Parameters(Vd=5V，T_A=+25℃)

Parameters	Min	Typ	Max	Unit
Frequency Range	40		53	GHz
Small Signal Gain		21		dB
Gain Flatness		±0.5		dB
Noise Figure		1.9		dB
P1dB		4		dBm
Input Standing Wave		1.8		-
Output Standing Wave		1.8		-
Static Current		13		mA

Use Restriction Parameters

Positive Drain Voltage	8V
Input Power	15dBm
Storage Temperature	-65℃~150℃
Operating Temperature	-55℃~85℃

External Dimensions

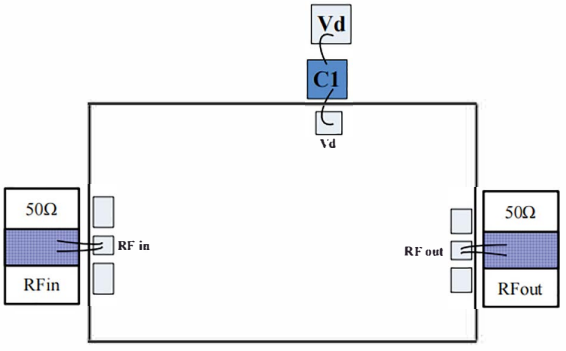


Note: 1) All dimensions marked are in micrometers (μm);
2) Dimensional tolerance for external dimensions: ± 50 μm;
3) The chip thickness is 70 μm.

Definition of Bonding Pressure Point

No.	Symbol	Function	Dimensions (μm^2)
1	RFin	RF signal input terminal, external 50 ohm system, no need for DC isolation capacitor	80×80
2	RFout	RF signal input terminal, external 50 ohm system, no need for DC isolation capacitor	80×80
3	Vd	The feeding end of the drain voltage requires an external 100pF bypass capacitor	100×100

Suggested Assembly Diagram



Note: The capacitance value of the peripheral capacitor C1 is 100 pF. It is recommended to use a single-layer capacitor and try to be as close as possible to the chip bonding point.

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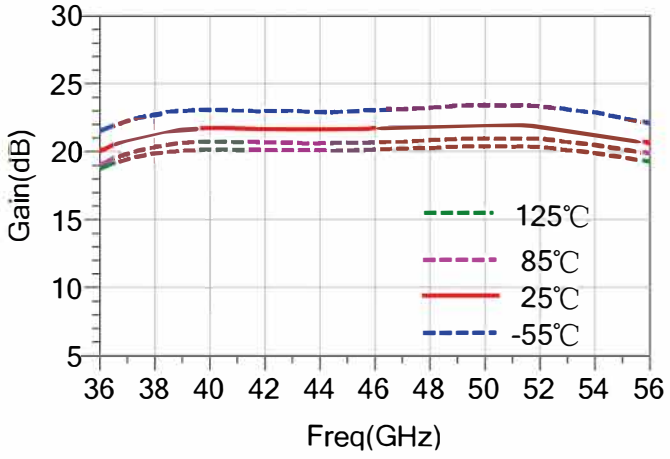
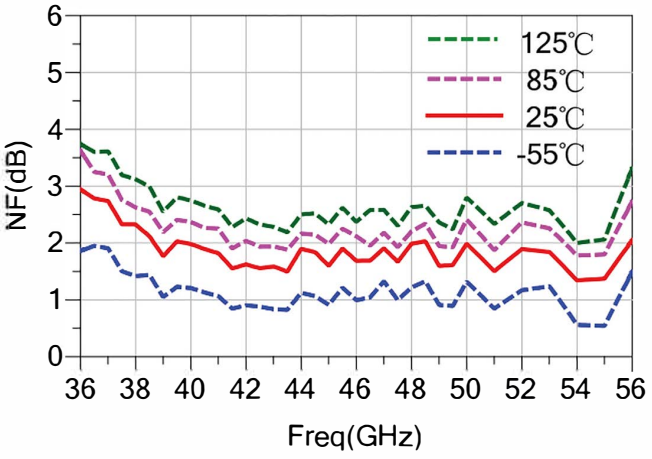
On Chip Testing Curve（Vd=5V，Id=13mA）

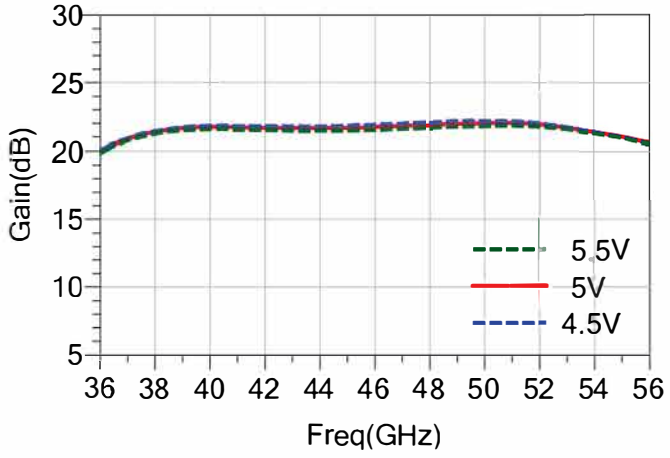
Small Signal Gain vs. Frequency



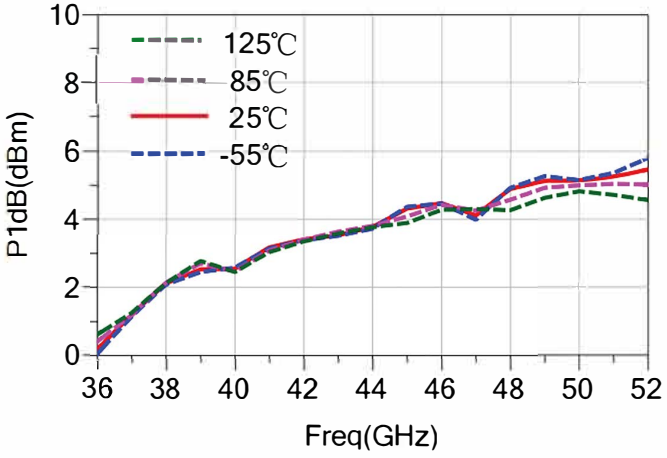
Noise Coefficient vs. Frequency



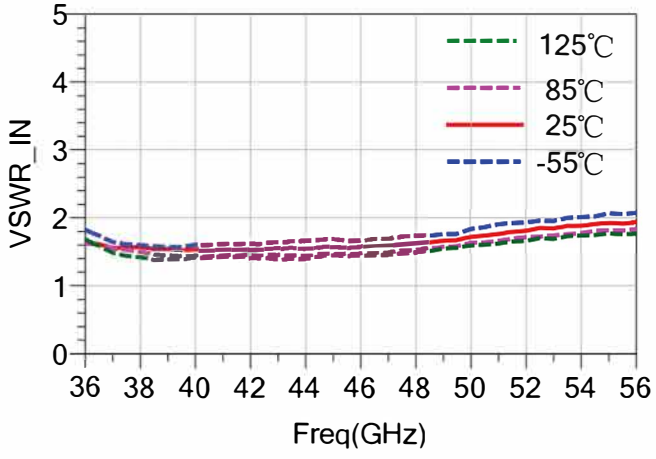
Small Signal Gain vs Voltage



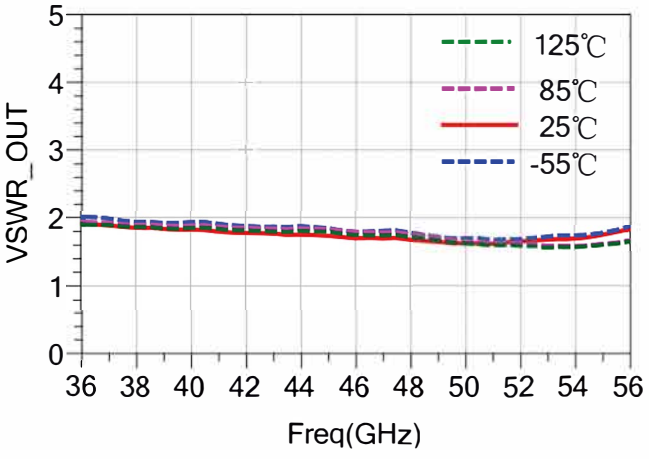
P1dB vs Frequency



Input Standing Wave vs. Frequency



Output Standing Wave vs. Frequency



Note:

1) Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.
3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
4) Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed tip. During the operation, avoid touching the chip surface with tools or fingers.
5) When powering on in sequence, apply gate voltage first and then drain voltage; When turning off the power, first remove the leakage voltage, and then remove the shed voltage.
6) Mounting operation: Chip installation can be carried out using AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
7) Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μm diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using as little ultrasonic energy as possible.
8) Please contact the supplier if you have any questions.