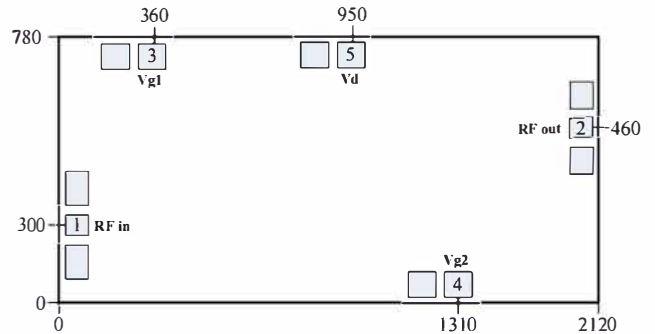


Performance Characteristics

- ✧ Frequency range: DC-75GHz
- ✧ Small signal gain: 12dB
- ✧ P1dB: 15dBm
- ✧ Noise factor: 5dB
- ✧ DC power supply: $V_d=8V$, $V_{g1}=1V$, $V_{g2}=-0.35V$, $I_d=95mA$
- ✧ Chip size: 2.12 mmx0.78 mmx0.07 mm

External External Dimensions



Note: 1) All dimensions marked are in micrometers (μm);
 2) Dimensional tolerance for external dimensions: $\pm 50 \mu m$;
 3) The chip thickness is 70 μm .

Product Introduction

Ultra wideband power amplifier chip, with a frequency range covering DC~75GHz, a typical small signal gain of 12dB, a typical P1dB of 15dBm, and a typical noise figure of 5dB.

Electrical Parameters ($V_d=8V$, $I_d=95mA$, $T_A=+25^\circ C$)

Parameters	Min	Typ	Max	Unit
Frequency Range	DC		75	GHz
Small Signal Gain		12		dB
P1dB		15		dBm
Noise Coefficient		5		dB
Gain flatness		± 1		dB
Input Standing Wave		1.8		-
Output Standing Wave		2	3	-
Saturation Current		100		mA

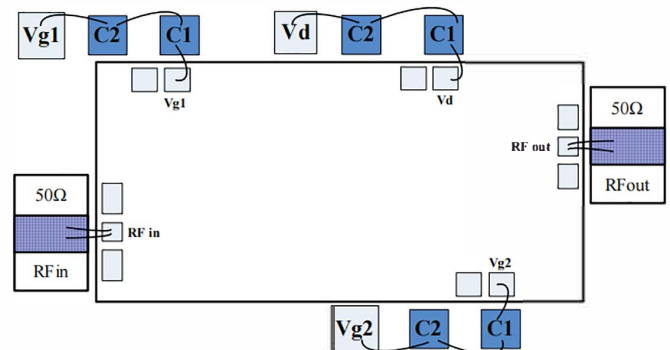
Definition of Bonding Pressure Point

No.	Symbol	Function	Dimensions (μm^2)
1	RFin	RF signal input terminal, connected to an external 50 ohm system, requires a DC isolation capacitor	80×70
2	RFout	RF signal input terminal, connected to an external 50 ohm system, requires a DC isolation capacitor	80×70
3、4	Vg1、Vg2	Gate voltage feeding terminal requires external 100pF and 10000pF bypass capacitors	120×120
5	Vd	The drain voltage feeding terminal requires external 100pF and 10000pF bypass capacitors	120×120

Use Restriction Parameters

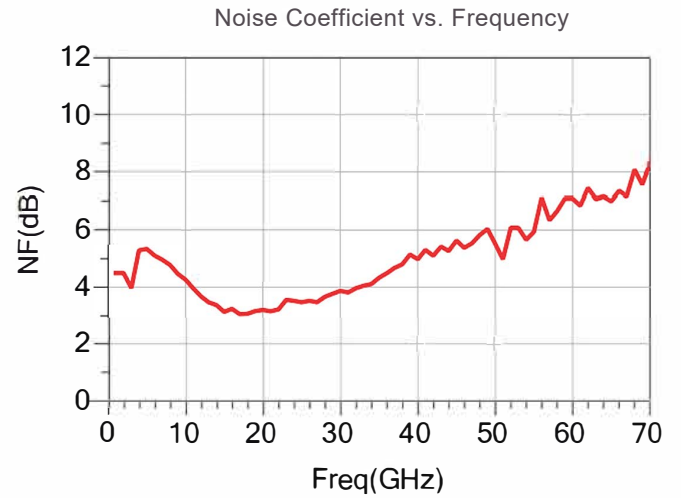
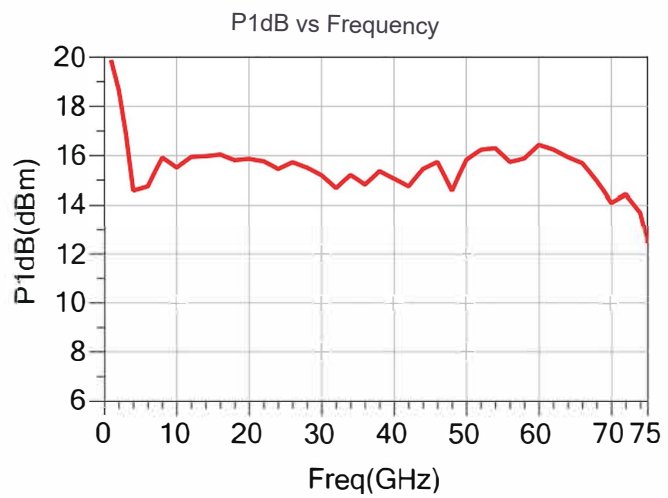
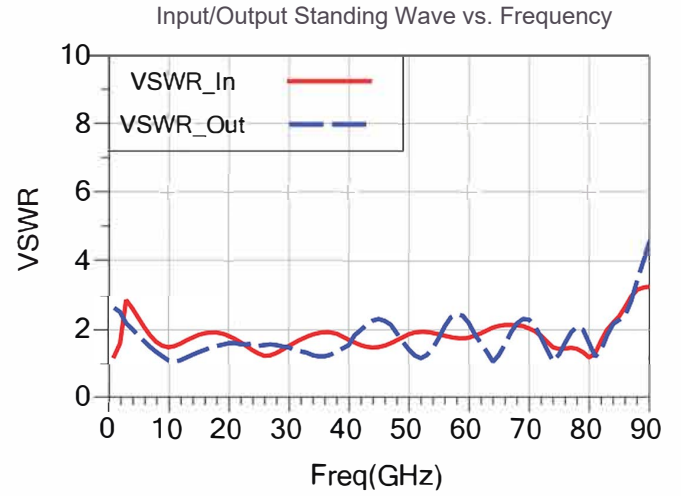
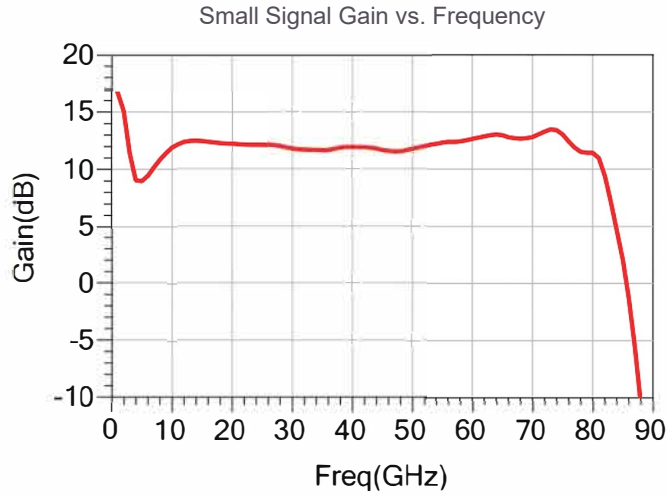
Negative gate voltage	-1V
Positive Drain Voltage	9V
Input Power	15dBm
Storage Temperature	$-65^\circ C \sim 150^\circ C$
Operating Temperature	$-55^\circ C \sim 85^\circ C$

Suggested Assembly Diagram



Note: 1) The capacitance of the peripheral capacitor C1 is 100 pF, and the capacitance of C2 is 10000 pF. It is recommended to use a single-layer capacitor for C1 and try to be as close to the chip bonding point as possible; Suggest adding 10 μF bypass capacitors to Vg and Vd.
 2) The input and output RF terminals require an external DC blocking capacitor.

On Chip Testing Curve ($T_A=+25^{\circ}\text{C}$) $V_d=8\text{V}$, $I_d=95\text{mA}$



Note:

- 1) Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
 - 2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.
 - 3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
 - 4) Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed tip. During the operation, avoid touching the chip surface with tools or fingers.
 - 5) When powering on in sequence, apply gate voltage first and then drain voltage; When turning off the power, first remove the leakage voltage, and then remove the shed voltage.
 - 6) Mounting operation: Chip installation can be carried out using AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
 - 7) Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μm diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using as little ultrasonic energy as possible.
 - 8) Please contact the supplier if you have any questions.
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