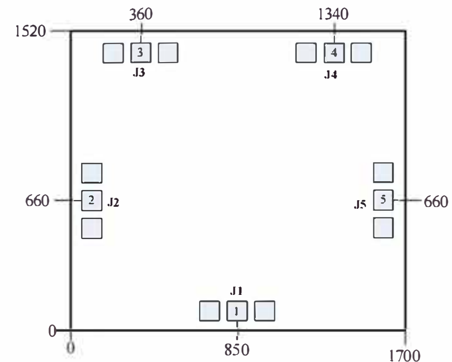
Performance Characteristics

- ✧ Frequency range：50MHz~50GHz
- ✧ With insertion loss：0.7dB@18GHz/1.2dB@50GHz(Typical values)
- ✧ Isolation degree：30dB(Typical values)
- ✧ Control current：Ic=-10mA@-1.4V(on)/+10mA@+ 1.4V(off)
- ✧ Chip size：1.70mmx1.52 mmx0.10 mm

Product Introduction

The broadband single pole four throw switch chip covers a frequency range of 50MHz~50GHz, with a typical insertion loss of 07dB, isolation greater than 30dB, and an RF input P1dB of 23dBm.

External Dimensions



Notes：

1) All dimensions marked are in micrometers (μm);
2) Dimensional tolerance for external dimensions: ±50μm;
3) The chip thickness is 100μm.

Electrical Performance Table(Von=-1.4V, Voff=+1.4V,T_A=+25°C)

Parameter	Min	Typ	Max	Unit
Frequency Range	0.05		50	GHz
With Insertion Loss	0.4	0.7	1.2	dB
Isolation Degree	25	30	40	dB
Amplitude Consistency		0.2		
Phase Consistency		10		
RF Input P1dB		23		dBm
Input Return Loss	-30	-15	-11	dB
Output Return Loss	-25	-20	-12	dB
Switching Time		20		ns

Definition Of Bonding Pressure Point

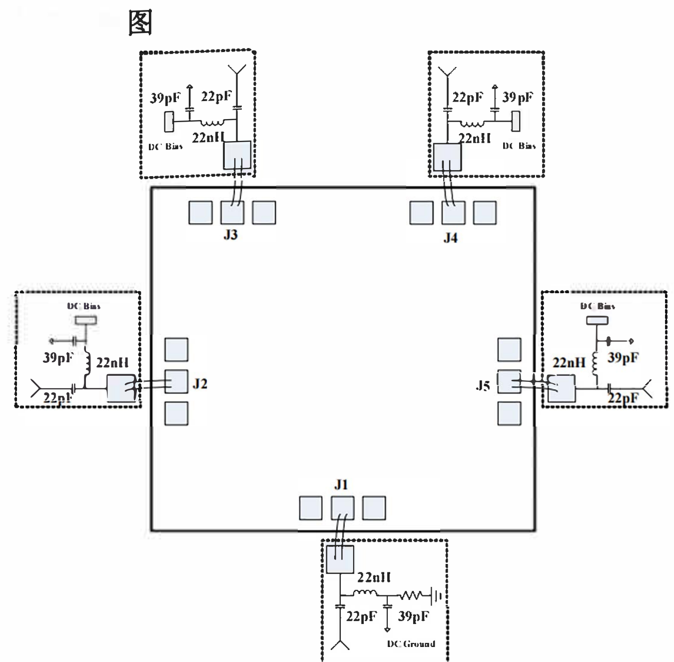
Number	Symbol	Function Description	Size (μm^2)
1	J1	RF signal input terminal, connected to an external 50 ohm system, requires a DC isolation capacitor.	100×100
2~5	J2~J5	RF signal output terminal, connected to an external 50 ohm system, requires a DC isolation capacitor.	100×100

Use Restriction Parameters

Input Power	23dBm
Bias Current	25mA
Storage Temperature	-65℃~150℃
Usage Temperature	-55℃~85℃

Suggested Assembly Diagram

图



Note: There is no DC blocking capacitor for input and output.

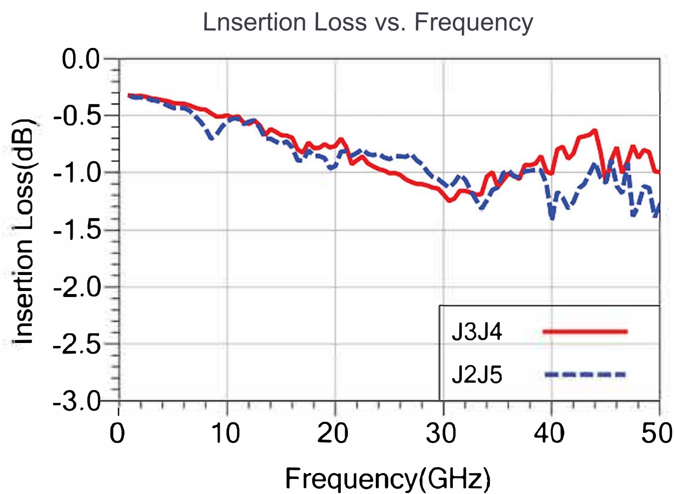
Truth Table

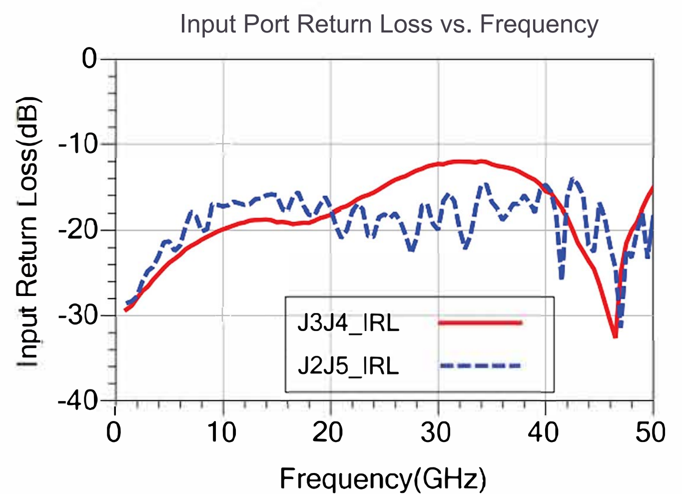
Control Input					On-off Status			
J1	J2	J3	J4	J5	J2-J1	J3-J1	J4-J1	J5-J1
GND	**-10mA**	+10mA	+10mA	+10mA	**On**	Off	Off	Off
GND	+10mA	**-10mA**	+10mA	+10mA	Off	**On**	Off	Off
GND	+10mA	+10mA	**-10mA**	+10mA	Off	Off	**On**	Off
GND	+10mA	+10mA	+10mA	**-10mA**	Off	Off	Off	**On**

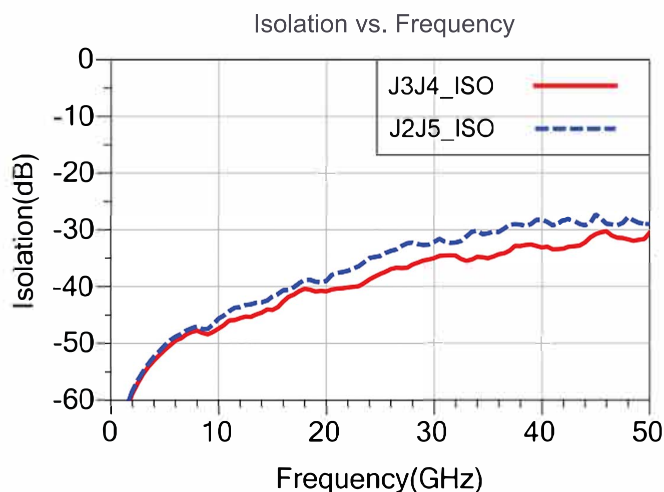
On Chip Testing Curve(TA=+25°c)

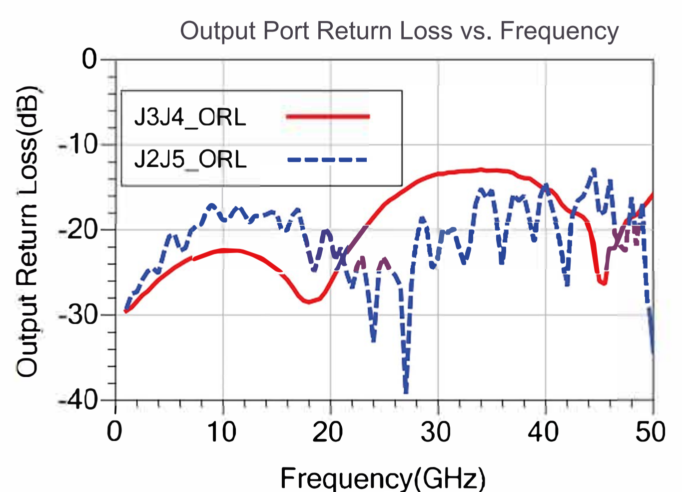
Freq_input=50MHz~50GHz, Pwr_Input=-15dBm;

The insertion loss and return loss are both test curves corresponding to the open state of the port









Note:

1)Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

2)Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.

3)Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.

4)Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed camera. During the operation, avoid touching the chip surface with tools or fingers.

5)Power on sequence: When powering on, apply gate voltage first, then drain voltage; When powering off, first remove the leakage voltage, then remove the gate voltage.

6)Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20 AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.

7)Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μ m diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using the smallest possible ultrasonic energy.

8)Please contact the supplier if you have any questions.