Performance Characteristics

- ✧ Frequency range：DC~67GHz
- ✧ Small signal gain：12dB
- ✧ P1dB： 16dBm
- ✧ Saturated output power：18dBm
- ✧ DC power supply：Vd=5V@Id=50mA(Vg≈-0.4V)
- ✧ Chip size：2.40 mmx1 .05 mmx0.07 mm

Product Introduction

The ultra wideband power amplifier chip covers a frequency range of DC~67GHz, with a typical small signal gain of 12dB and a typical saturated output power of 18dBm.

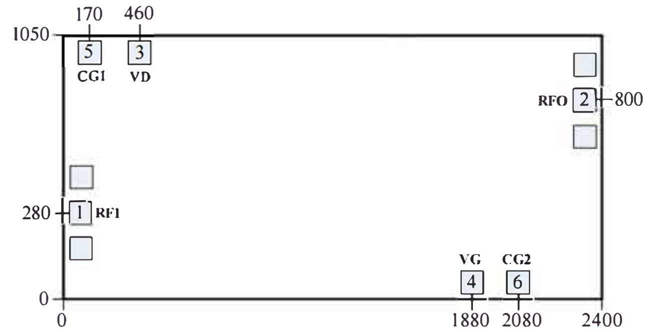
Electrical Performance Table (Vd=5V, Id=50mA, T_A=+25 °C)

Parameter	Min	Typ	Max	Unit
Frequency Range	DC		67	GHz
Small Signal Gain		12		dB
Gain Flatness		±0.5		dB
Noise Coefficient		4		dB
P1dB		16		dBm
Saturated Output Power		18		dBm
Input Return Loss		-17		dB
Output Return Loss		-13		dB
Static Current		50		mA

Use Restriction Parameters

Drain Voltage(Vd)	+6V
Gate Voltage(Vg)	-4V
Input Power	20dBm
Storage Temperature	-65℃~150℃
Usage Temperature	-55℃~85℃

External Dimensions



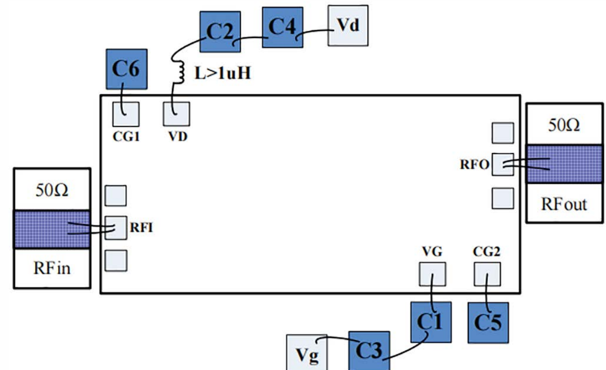
Notes：

1) All dimensions marked are in micrometers (μm);
2) Dimensional tolerance for external dimensions: ±50μm;
3) The chip thickness is 70μm.

Definition Of Bonding Pressure Point

Number	Symbol	Function Description	Size(μm^2)
1	RFI	RF signal input terminal, externally connected to a 50 ohm system, requiring an external DC blocking capacitor	90×80
2	RFO	RF signal output terminal and drain voltage feeding terminal require external DC blocking capacitors	90×80
3	VD	The drain voltage feeding terminal requires an external 1000pF and 0.1 μ F bypass capacitor	100×100
4	VG	Gate voltage feeding terminal requires external 1000pF and 0.1 μ F bypass capacitors	100×100
5	CG1	Low frequency expansion port with drain, requiring an external 0.1 μ F capacitor	100×100
6	CG2	Gate low-frequency expansion port, requiring an external 0.1 μ F capacitor	100×100

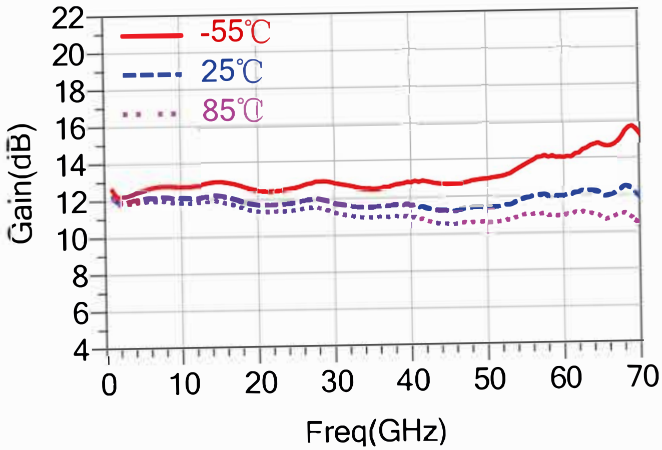
Suggested Assembly Diagram

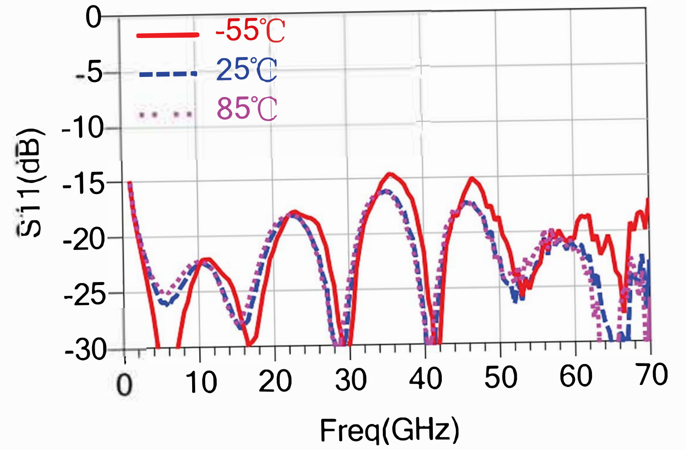


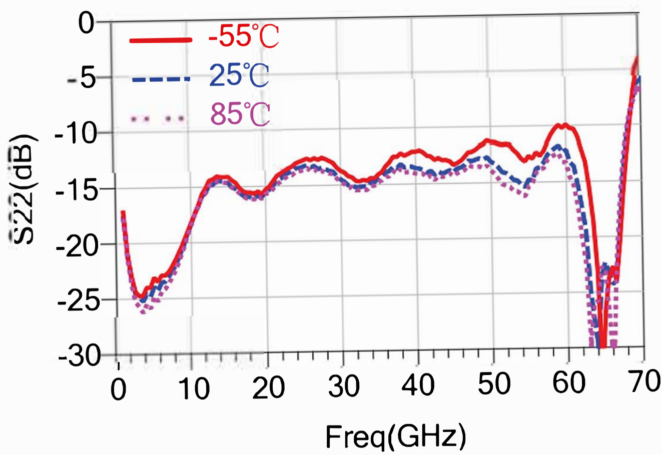
Notes:

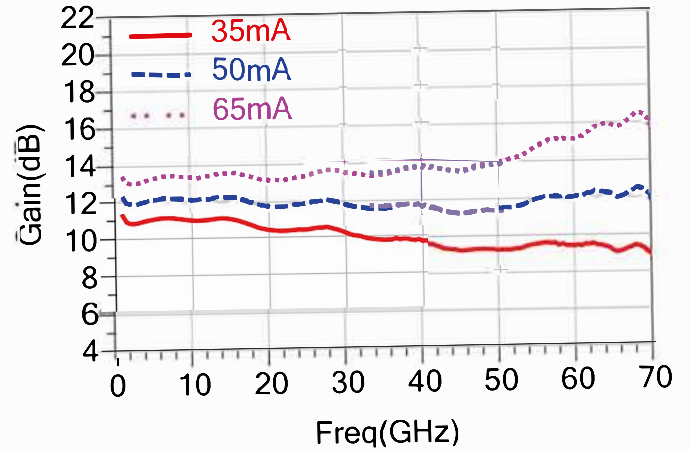
The capacitance values of the peripheral capacitors C1~C2 are 1000pF, and the capacitance values of C3~C6 are 0.1uF. It is recommended to use single-layer capacitors for C1~C2, and C1 should be as close as possible to the chip bonding point.

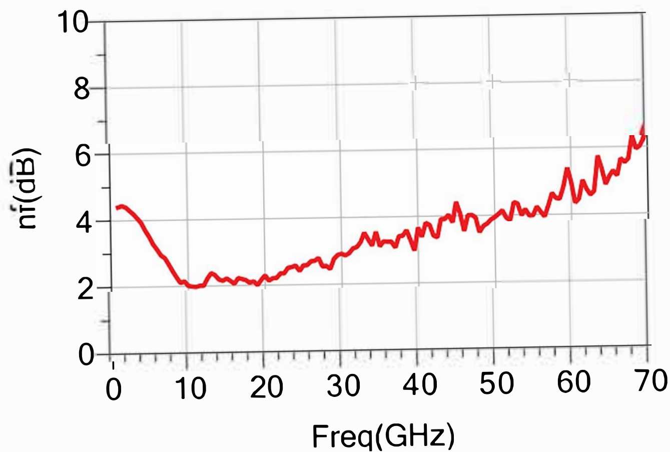
On chip testing curve

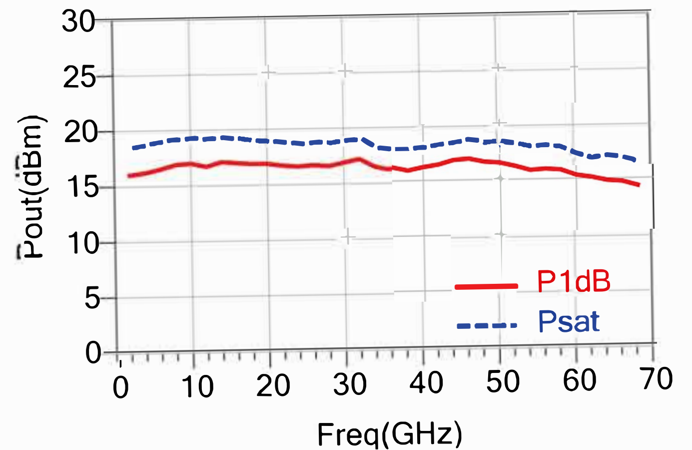












Note:

1)Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

2)Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.

3)Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.

4)Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed camera. During the operation, avoid touching the chip surface with tools or fingers.

5)Power on sequence: When powering on, apply gate voltage first, then drain voltage; When powering off, first remove the leakage voltage, then remove the gate voltage.

6)Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20 AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.

7)Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μ m diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using the smallest possible ultrasonic energy.

8)Please contact the supplier if you have any questions.