Standard Circuit

GPA-0050
Power Amplifier Chip

Performance Characteristics

Frequency range: DC-50GHz
Small signal gain: 12dB
P1dB: 16dBm
Saturation output power: 18dBm
DC Power: Vd=5V@Id=50mA(Vg≈-0.4V)
Size: 2.00 mmxl .05 mmx0.07 mm

Product Introduction

Ultra wideband power amplifier chip, with a frequency range covering DC~50GHz, a typical small signal gain of 12dB, and a typical saturated output power of 18dBm.

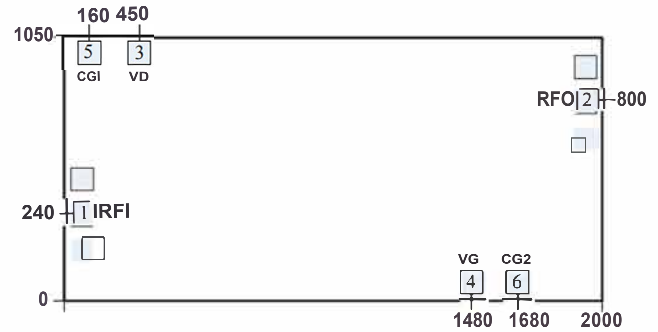
Electrical Performance(Vd=5V, Id=50mA, T_A=+25°C)

Index	Min	Typ	Max	Unit
DC Input Frequency			50	GHz
Small signal gain		12		dB
Gain flatness		± 05		dB
Noise Figure		3		**dB**
P1dB		16		dBm
Saturation Output Power		18		dBm
Input Return Loss		-17		dB
Output Return Loss		-13		dB
Quiescent Current		50		mA

Use Restriction Parameters

Drain voltage (Yd)	+6V
Gate voltage (Vg)	-4V
Input power	20dBm
Storage Temperature	-65°C~l50°C
Operating Temperature	-55°C~85°C

External Dimensions

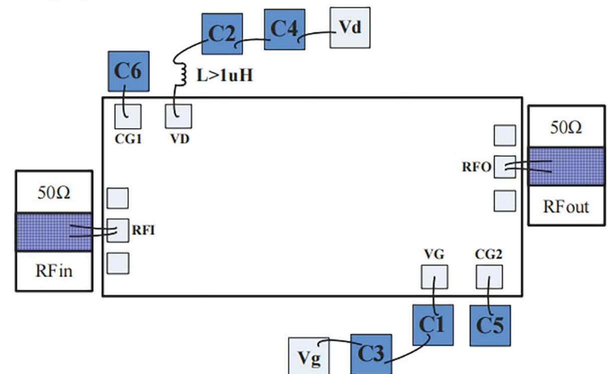


Note: 1) All dimensions marked are in micrometers (μm);
2) Dimensional tolerance for external dimensions: ±50μm;
3) The chip thickness is 70 μm.

Bonding Pressure Point Definition

No.	Symbol	Function	Size(μm²)
I	RFI	RF signal input terminal, externally connected to a 50 ohm system, requiring an external DC blocking capacitor	90X90
2	RFO	RF signal output terminal and drain voltage feeding terminal require external DC blocking capacitors	90X90
3	VD	The drain voltage feeding terminal requires external IOOOpF and 0lμ F bypass capacitors	IOOX 100
4	VG	Gate voltage feeding terminal requires external IOOOpF and 0lμF bypass capacitors	IOOX 100
5	CG!	Low frequency expansion port with drain, requiring an external 0 l μ F capacitor	IOOX 100
6	CG2	Gate low-frequency expansion port requires an external 0 l μ F capacitor	IOOX 100

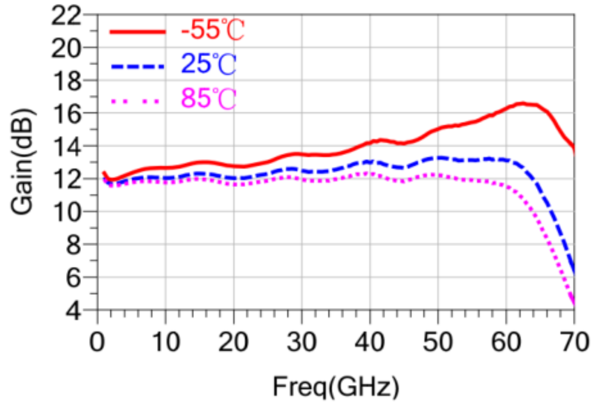
Suggested Assembly Diagram



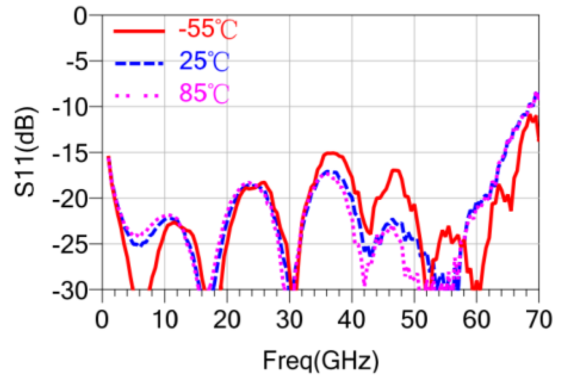
Note: The capacitance value of the peripheral capacitor CI-C2 is 1000 pF, and the capacitance value of C3-C6 is 01 uF. It is recommended to use single-layer capacitors for CI~C2, and CI should be as close as possible to the chip bonding pressure point.

On Chip Testing Curve

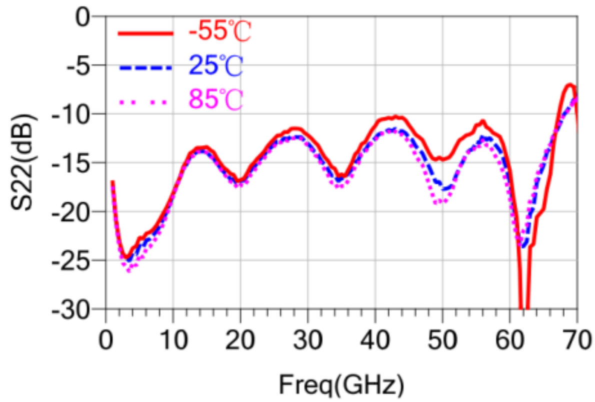
Small Signal Gain vs. Frequency



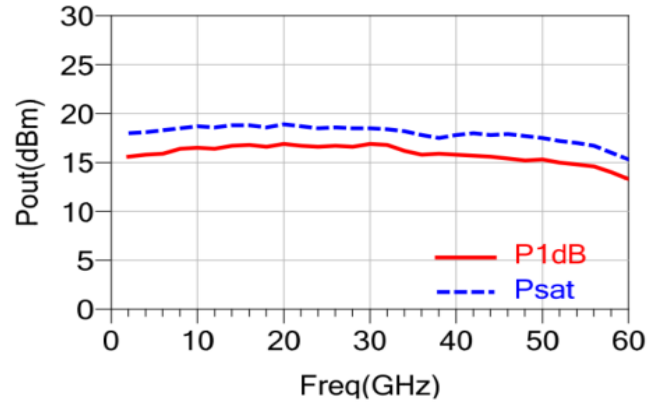
Input Return Loss vs. Frequency



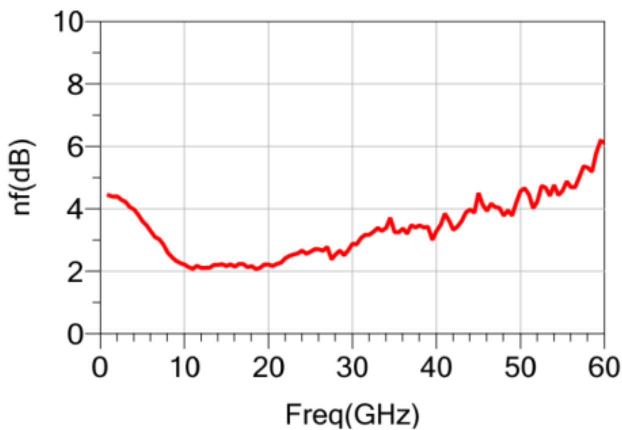
Output Return Loss vs. Frequency



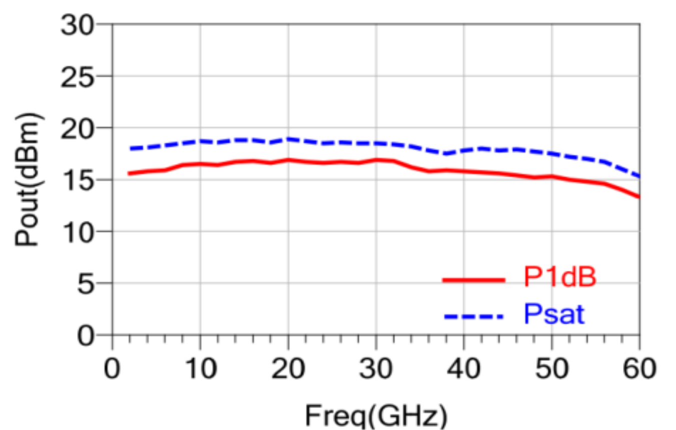
Small Signal Gain vs. Frequency@T_A=25℃



Noise Efficient vs. Frequency@T_A=25℃



Output Power vs. Frequency@T_A=25℃



Note:

l) Storage: The chip must be placed in a container with electrostatic protection function,And store it in a nitrogen environment.

2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.

3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.

4) Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed tip. During the operation, avoid touching the chip surface with tools or fingers.

5) Power on sequence: When powering on, apply voltage first, then apply leakage voltage; When turning off the power, first remove the leakage voltage, and then remove the shed voltage.

6) Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.

Sintering process: Use 80/20AuSn for sintering, with a sintering temperature not exceeding 300'C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.

Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.

7) Keying operation:

Unless otherwise specified, use 2 bonding wires (25 μ m diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.

Hot ultrasonic bonding temperature is 150 ° C, using the smallest possible ultrasonic energy.

8) Please contact the supplier if you have any questions.