Standard Circuit

GPA-3464
Power Amplifier Chip

Performance Characteristics

- ✧ Frequency range： 34GHz~64GHz
- ✧ Small signal gain： 19dB
- ✧ Saturated output power： 27dBm
- ✧ DC power supply： Vd=4V@Id=810mA(Vg=-0.4V)
- ✧ Chip size： 3.90 mmx2.30 mmx0.07 mm

Product Introduction

A broadband power amplifier chip covering Q and U bands, with a frequency range of 34GHz~64GHz, a typical small signal gain of 19dB, a typical saturated output power of 27dBm, and a typical additional efficiency of 17%.

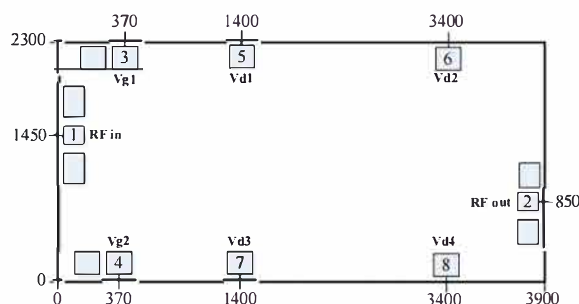
Electrical Performance Table (Vd=4V, Id=810mA, TA=+25°C)

Parameter	Min	Typ	Max	Unit
Frequency Range	34		64	GHz
Small Signal Gain		19		dB
Gain Flatness		±1.5		dB
Saturated Output Power		27		dBm
Power Added Efficiency		17		%
Power Gain		17		dB
Input Standing Wave		1.5		-
Output VSWR		1.5		-
Saturation Current		870		mA

Use Restriction Parameters

Negative Gate Voltage	-1V
Positive Drain Voltage	6V
Input Power	20dBm
Storage Temperature	-65℃~150℃
Usage Temperature	-55℃~85℃

External Dimensions



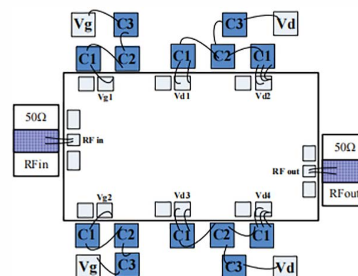
Notes：

1) All dimensions marked are in micrometers (μm);
2) Dimensional tolerance for external dimensions: ±50μm;
3) The chip thickness is 70μm.

Definition Of Bonding Pressure Point

Number	Symbol	Function Description	Size(μm^2)
1	RFin	RF signal input terminal, external 50 ohm system, no need for DC isolation capacitor	80×80
2	RFout	RF signal output terminal, external 50 ohm system, no need for DC isolation capacitor	80×80
3、4	Vg1、Vg2	Gate voltage feeding terminal requires external 100pF, 10000pF, and 10uF bypass capacitors	120×120
5、6、7、8	Vd1、Vd2、Vd3、Vd4	The drain voltage feeding terminal requires external 100pF, 10000pF, and 10uF bypass capacitors	120×120

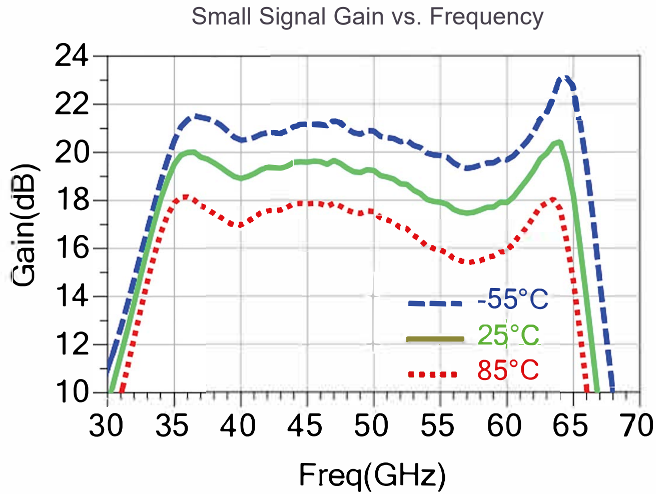
Suggested Assembly Diagram

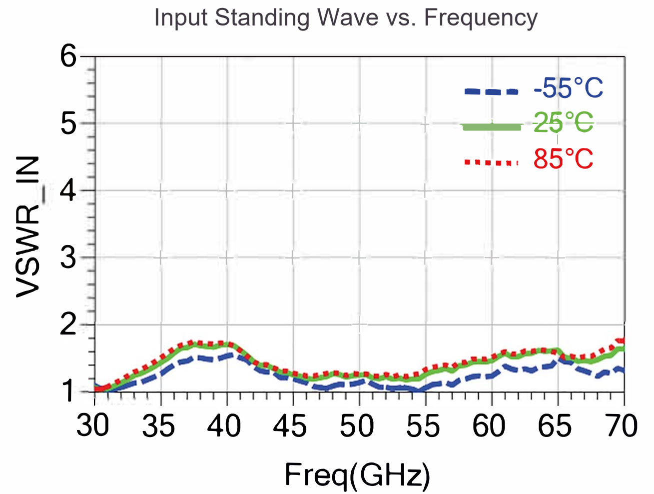


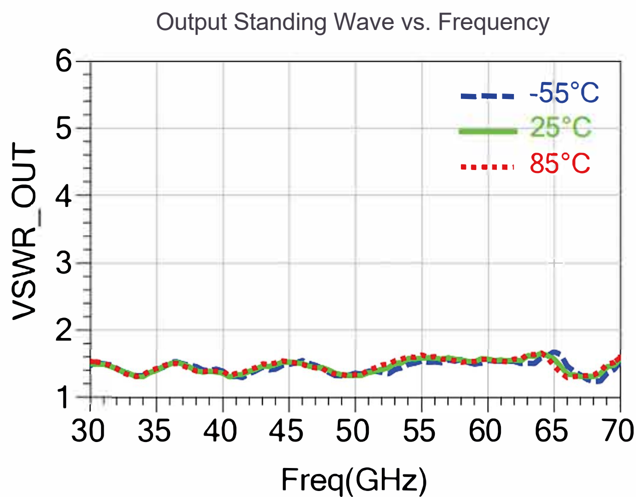
Notes:

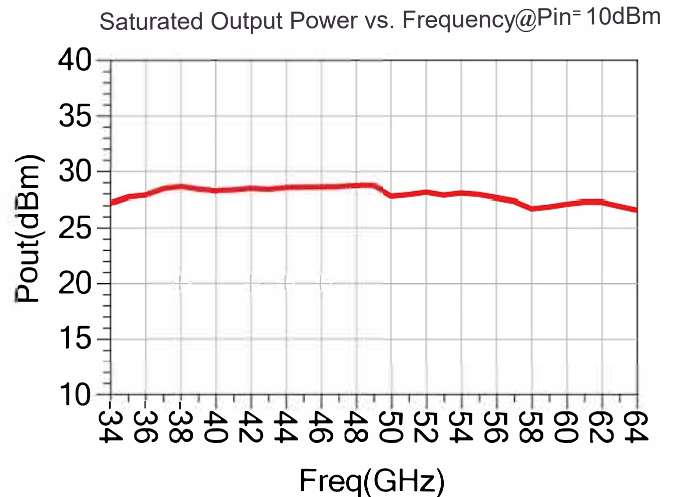
1) The capacitance of the peripheral capacitor C1 is 100 pF, the capacitance of C2 is 10000 pF, and the capacitance of C3 is 10 μf. It is recommended to use a single-layer capacitor for C1 and try to be as close to the chip bonding point as possible.
2) Vg1 and Vg2 only need to be biased together.

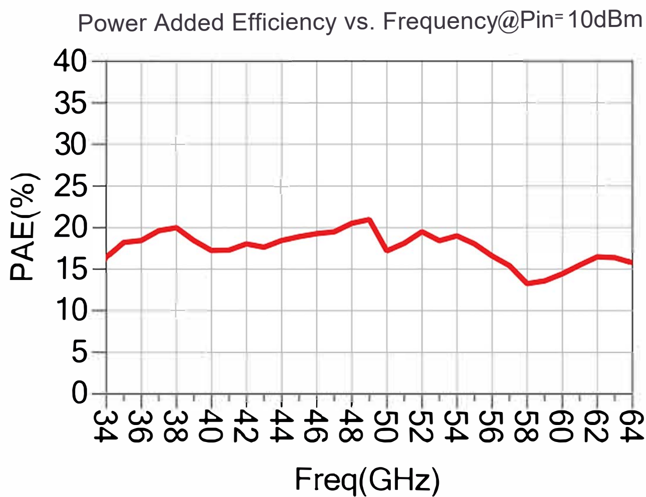
On Chip Pulse Test Curve(T_A=+25°c) Vd=4V, Id=810mA

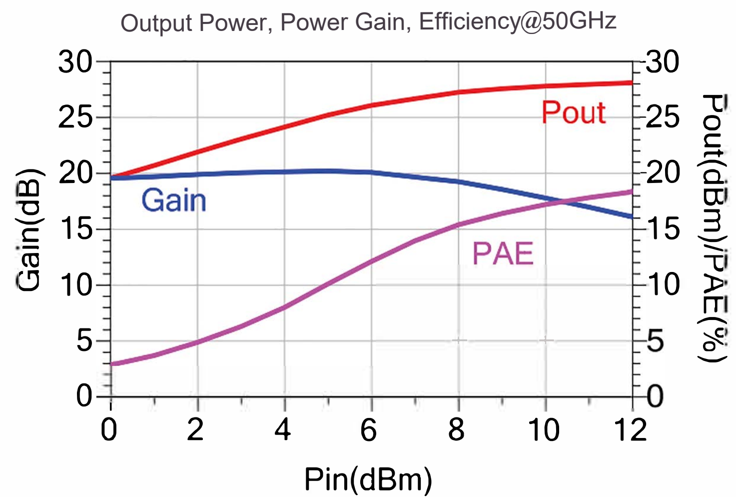












Note:

1) Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.

3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.

4) Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed camera. During the operation, avoid touching the chip surface with tools or fingers.

5) Power on sequence: When powering on, apply gate voltage first, then drain voltage; When powering off, first remove the leakage voltage, then remove the gate voltage.

6) Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20 AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.

7) Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μ m diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using the smallest possible ultrasonic energy.

8) Please contact the supplier if you have any questions.