

Performance Characteristics

- ✧ Frequency range : DC~125GHz
- ✧ Typical values of linear gain:10dB@DC~110GHz, 7dB@110~125GHz
- ✧ DC power supply: Yd=45V@Id=48mA(Vg1=-0.4V,Vg2=1.1V)
- ✧ Chip size: 1.70mmx1.00 mmx0.07 mm

Product Introduction

Ultra wideband power amplifier chip, with a frequency range covering DC~125GHz. The typical value of DC~110GHz linear gain is better than 10dB, and the typical value of reverse isolation is better than 30dB. The typical value of linear gain for 110-125GHz is 7dB, and the typical value of reverse isolation is 30dB.

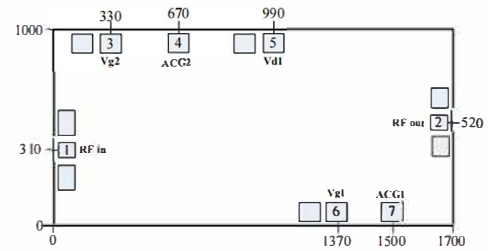
Electrical performance table(Vd=4.5V, Id=48mA, TA=+25°C)

Parameter	Typ				Unit
	DC-70	70-90	90-110	110-125	
Frequency Range					GHz
Linear Gain	10	12	10	7	dB
Reverse Isolation	35	35	30	30	dB
Noise Coefficient	4		5		dB
PI _{dB}	10	7	3	0	dBm
Saturated Power	12	10	7	3	dBm
Input Standing Wave	2				-
Output VSWR	2				-
Saturation Current	60				mA

Use Restriction Parameters

Negative Gate Voltage	-1V
Positive Drain Voltage	5V
Input Power	10dBm
Storage Temperature	-65°C~150°C
Usage Temperature	-55°C~85°C

External Dimensions



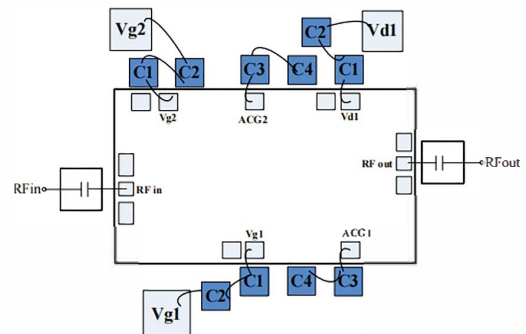
Notes:

- 1) All dimensions marked are in micrometers (μm);
- 2) Dimensional tolerance for external dimensions: $\pm 50\mu\text{m}$;
- 3) The chip thickness is $70\mu\text{m}$.

Definition Of Bonding Pressure Point

Number	Symbol	Function Description	Size(μm^2)
1	RF in	RF signal input terminal, connected to an external 50 ohm system, requires the addition of Bias Tee or DC blocking capacitor	80×80
2	RF out	RF signal output terminal, connected to an external 50 ohm system, requires the addition of BiasTree or DC blocking capacitor	80×80
3、6	Vg2、Vg1	Gate voltage feeding terminal requires external 100pF and 0.01uF bypass capacitors	100×100
4、7	ACG2、ACG1	Low frequency terminal requires external 1000pF and 0.47uf bypass capacitors	100×100
5	Vd1	The drain voltage feeding terminal requires an external 100pF and 0.01uf bypass capacitor	100×100

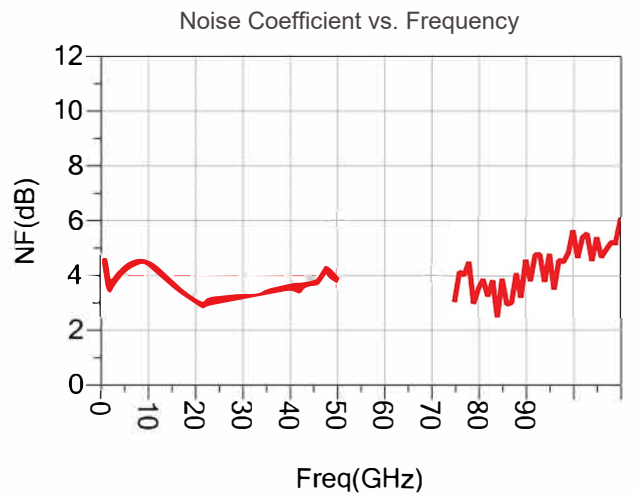
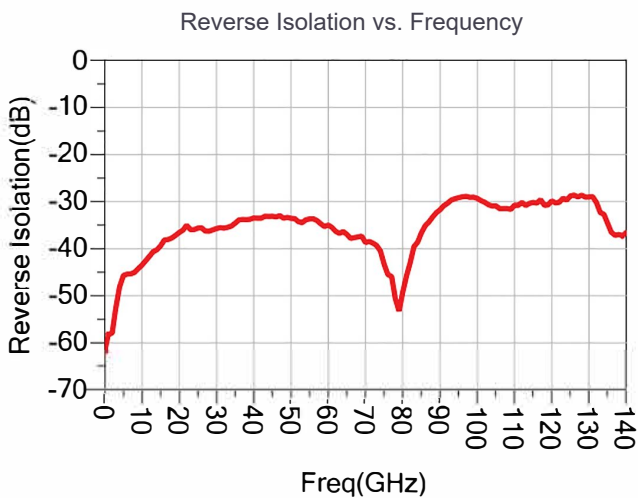
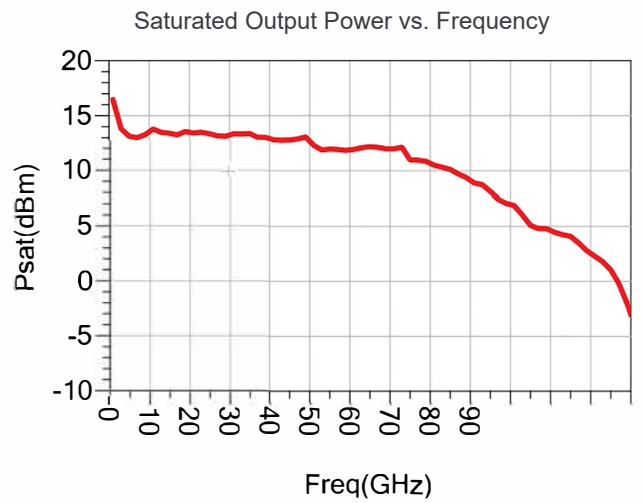
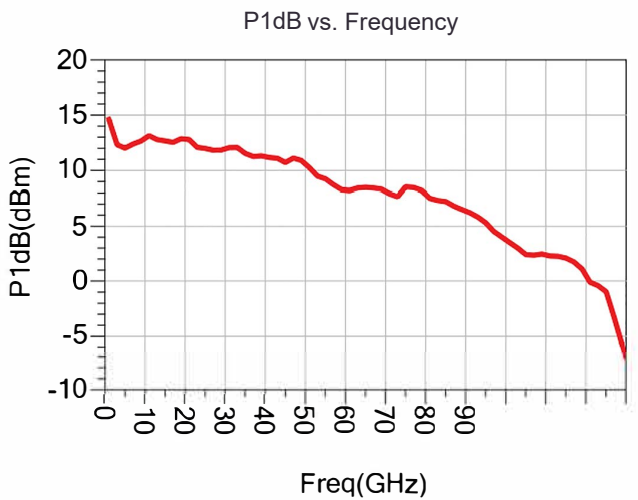
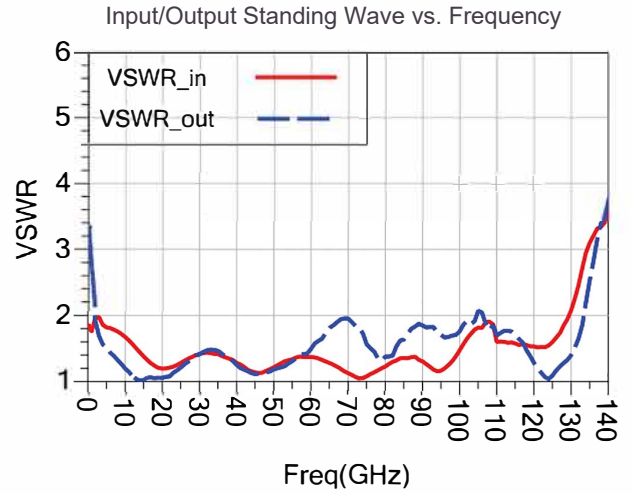
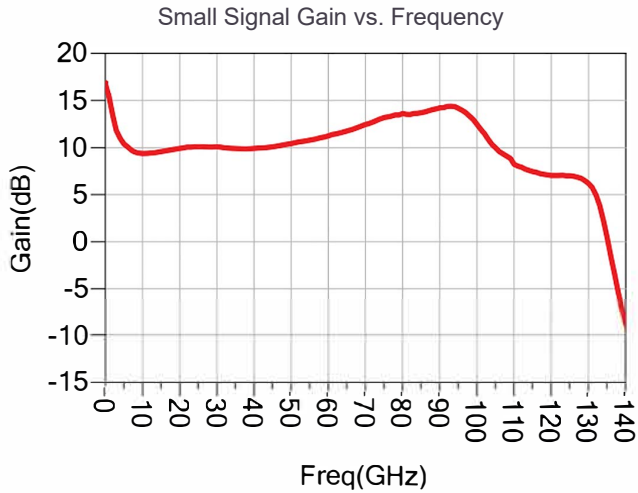
Suggested Assembly Diagram



Notes :

- 1) The capacitance of the peripheral capacitor C1 is 100pF, the capacitance of C2 is 0.01 μF , the capacitance of C3 is 1000pF, and the capacitance of C4 is 0.47 μF . Among them, it is recommended to use a single-layer capacitor for C1 and try to be as close as possible to the chip bonding point. Suggest adding a 10 μF bypass capacitor to Vg and Vd.

Continuous Wave Test Curve In Film



Note:

- 1) Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
 - 2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.
 - 3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
 - 4) Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed camera. During the operation, avoid touching the chip surface with tools or fingers.
 - 5) Power on sequence: When powering on, apply gate voltage first, then drain voltage; When powering off, first remove the leakage voltage, then remove the gate voltage.
 - 6) Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20 AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
 - 7) Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μ m diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using the smallest possible ultrasonic energy.
 - 8) Please contact the supplier if you have any questions.
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