Standard Circuit

GPA-3075
Power Amplifier Chip

Performance Characteristics

- ✧ Frequency range ： 30GHz~75GHz
- ✧ Small signal gain： 20dB
- ✧ Saturated output power： 21dBm@8%PAE
- ✧ P1dB：20dBm
- ✧ DC power supply： Vd=4V@Id=250mA (Vg=-0.35V)
- ✧ Chip size： 3.6 mmx1.7 mmx0.07 mm

Product Introduction

A broadband power amplifier chip covering the Ka band to U band, with a frequency range of 30GHz~75GHz, a typical small signal gain of 20dB, and a typical saturated output power of 21dBm.

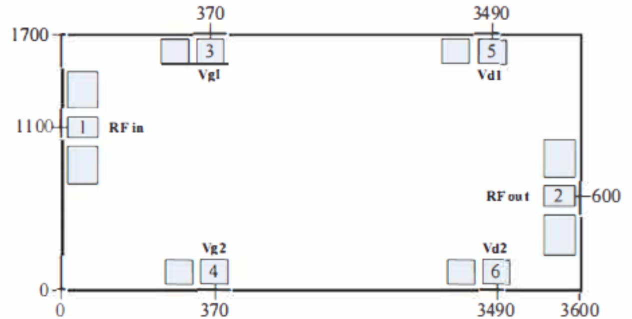
Electrical Performance Table(Vd=4V, Id=250mA，T_A=+25°C)

Parameter	Min	Typ	Max	Unit
Frequency Range	30		75	GHz
Small Signal Gain		20		dB
Gain Flatness		±2		dB
PldB		20		dBm
Saturated Output Power		21		dBm
Power Added Efficiency		8		%
Input Standing Wave		1.6		
Output VSWR		1.6		
Saturation Current		480		mA

Use Restriction Parameters

Negative Gate Voltage	-1V
Positive Drain Voltage	4.5V
Input Power	15dBm
Storage Temperature	-65℃~150℃
Usage Temperature	-55℃~85℃

External Dimensions



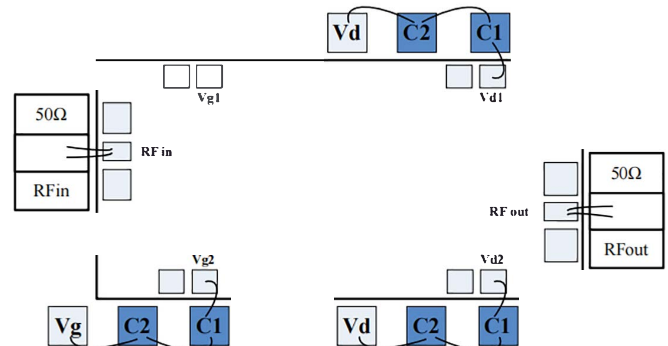
Notes：

1) All dimensions marked are in micrometers (μm);
2) Dimensional tolerance for external dimensions: ±50μm;
3) The chip thickness is 70μm.

Definition Of Bonding Pressure Point

Number	Symbol	Function Description	Size(μm^2)
	Rfm	RF signal input terminal, external 50 ohm system, no need for DC isolation capacitor	100×80
2	RFout	RF signal output terminal, external 50 ohm system, no need for DC isolation capacitor	100×80
3、4	Vgl、Yg2	Gate voltage feeding terminal requires external 100pF and 10000pF bypass capacitors	120×120
5、6	Ydl、Vd2	The drain voltage feeding terminal requires external 100pF and 10000pF bypass capacitors	120×120

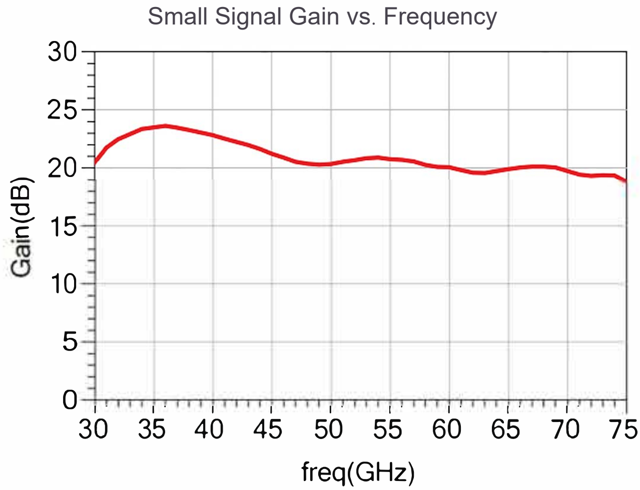
Suggested Assembly Diagram

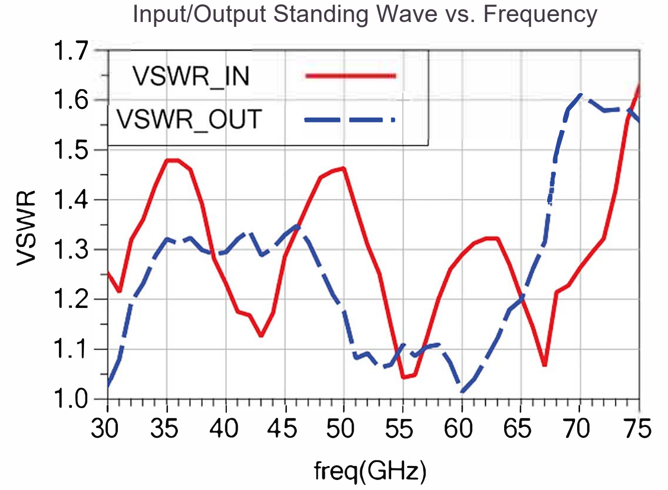


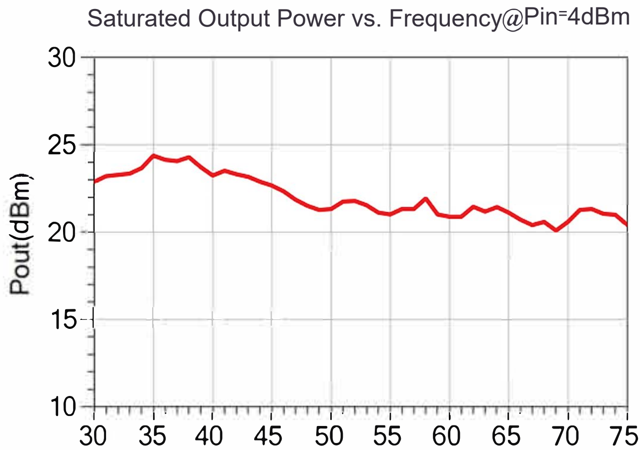
Notes:

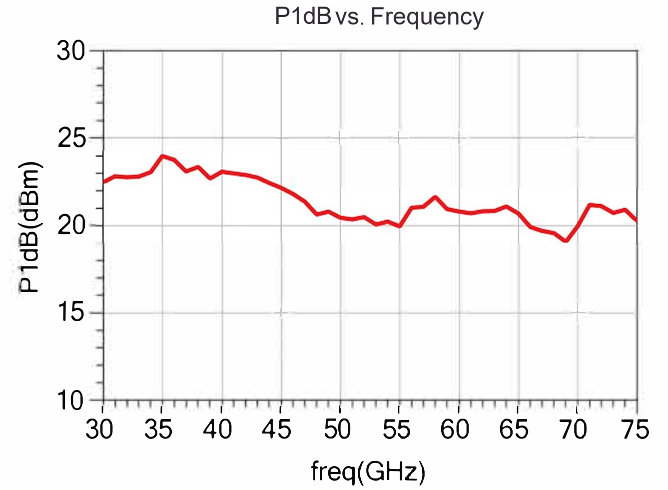
1)Vg1 and Vg2 only need to be bonded to one pressure point.
2)The capacitance of the peripheral capacitor C1 is 100pF, and the capacitance of C2 is 10000pF. It is recommended to use a single-layer capacitor for C1 and try to be as close as possible to the chip bonding point. Suggest adding 10 μF bypass capacitors to Vg and Vd.

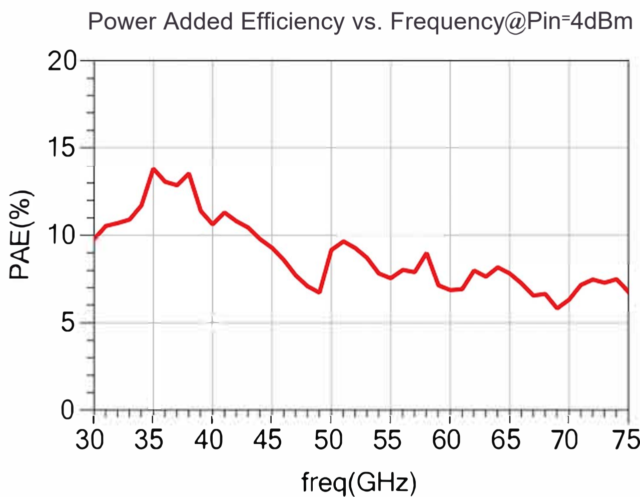
On Chip Testing Curve (TA=+25°C) Vd=4V, Id=400mA

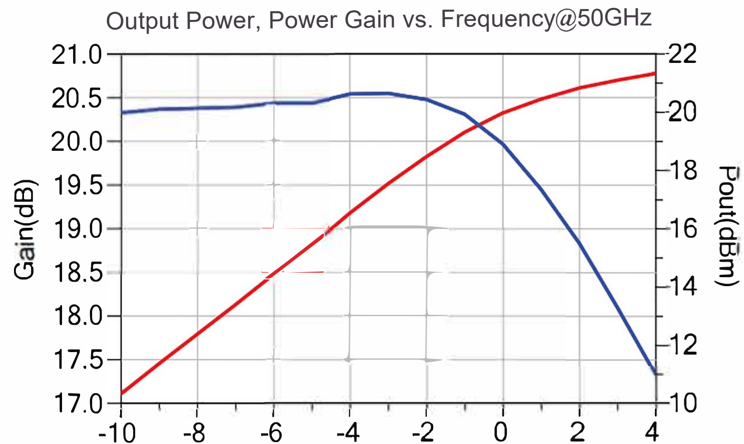












Note:

1） Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

2） Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.

3） Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.

4） Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed camera. During the operation, avoid touching the chip surface with tools or fingers.

5） Power on sequence: When powering on, apply gate voltage first, then drain voltage; When powering off, first remove the leakage voltage, then remove the gate voltage.

6） Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20 AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.

7） Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μ m diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using the smallest possible ultrasonic energy. The pressure of the spherical bonding chopper is 40-50 gf, and the pressure of the wedge-shaped bonding chopper is 18-22 gf.

8） Please contact the supplier if you have any questions.