

Performance Characteristics

- ♦ Frequency range : 20GHz~50GHz
- ♦ Small signal gain : 26dB
- ♦ Saturated output power : 24dBm@13%PAE
- ♦ PldB: 23dBm
- \diamond DC power supply : Vd=4V@Id=400mA (Vg=-0.35V)
- ♦ Chip size : 3.5 mm×1.7 mm×0.07 mm

Product Introduction

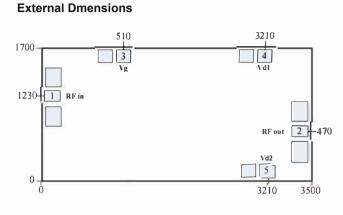
The Ka band broadband power amplifier chip covers a frequency range of 20GHz-50GHz, with a typical small signal gain of 26dB and a typical saturated output power of 24dBm.

Electrical Performance	Table(Vd=4V,	Id=400rnA,	T _A =+25°C)
------------------------	--------------	------------	------------------------

Parameter	Min	Тур	Max	Unit
Frequency Range	20		50	GHz
Small Signal Gain		26		dB
Gain Flatness		±2		dB
PldB		23		dBm
Saturated Output Power		24		dBm
Power Added Efficiency		13		%
Input Standing Wave		1.5		2 2 (
Output VSWR		1.5		æ
Saturation Current		600		mA

Use Restriction Parameters

Negative Gate Voltage	-1V
Positive Drain Voltage	4.5V
Input Power	15dBm
Storage Temperature	-65℃~150℃
Usage Temperature	-55℃~85℃



Notes :

1) All dimensions are in micrometers(µm);

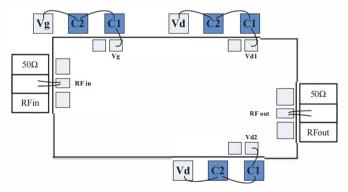
 Dimensional tolerances for external dimensions of length and width: ±50µm;

3) Chip thickness70µm.

Definition Of Bonding Pressure Point

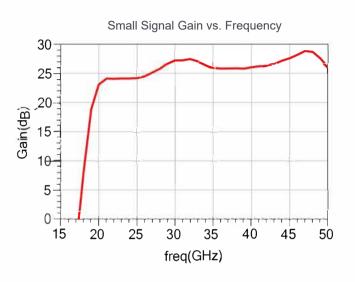
Number	Symbol	Function Description	Size(µm²)
1	Rfm	RF signal input terminal, external 50 ohm system, no need for DC isolation capacitor	100×80
2	RFout	RF signal output terminal, external 50 ohm system, no need for DC isolation capacitor	100×80
3	Vg	Gate voltage feeding terminal requires external 100pF and 10000pF bypass capacitors	120×120
4、5	Vd 1、Vd2	The drain voltage feeding terminal requires external 100pF and 10000pF bypass capacitors	120×120

Suggested Assembly Diagram

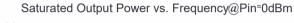


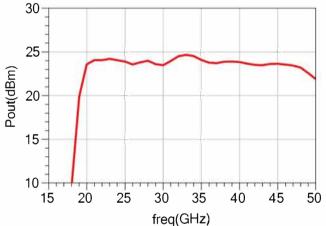
Notes : The capacitance of the peripheral capacitor C1 is 100 pF, and the capacitance of C2 is 10000 pF. It is recommended to use a single-layer capacitor for C1 and try to be as close as possible to the chip bonding point. Suggest adding 10 μ F bypass capacitors to Vg and Vd.

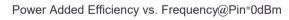


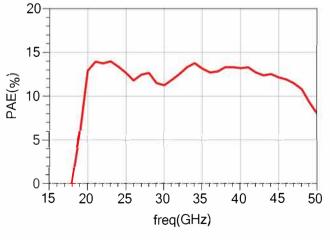


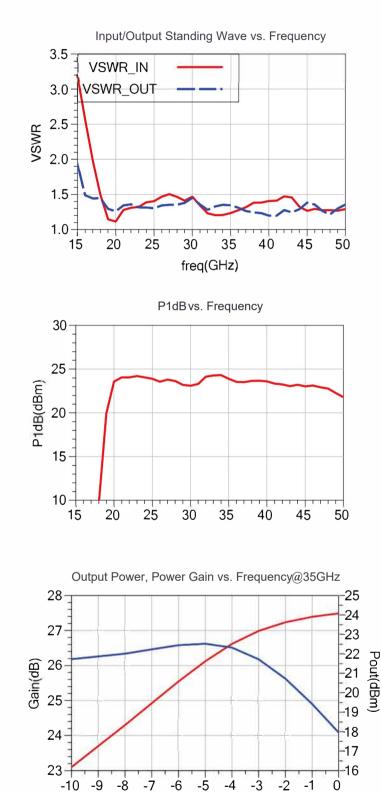
On Chip Testing Curve(TA=+25°C) Vd=4V, Id=400mA











freq(GHz)



Note:

1) Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.

2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and liquid cleaning agents are prohibited from cleaning the chips.

3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.

4) Conventional operation: To retrieve the chip, please use a vacuum chuck or precision pointed punch. During the operation, avoid touching the chip surface with tools or fingers.

5) Power on sequence: When powering on, apply gate voltage first, then drain voltage; When powering off, first remove the leakage voltage, then remove the gate voltage.

6) Mounting operation: Chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.

Sintering process: Use 80/20 AuSn for sintering, with a sintering temperature not exceeding 300°C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds. Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.

7) Keying operation:

Unless otherwise specified, use 2 bonding wires (25 µm diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.

Hot ultrasonic bonding temperature is 150°C, using the smallest possible ultrasonic energy. The pressure of the spherical bonding chopper is 40-50 gf, and the pressure of the mold bonding chopper is 18-22 gf.

8) Please contact the supplier if you have any questions.