

GaAs MMIC SPDT Reflective Switch Chip, DC-50GHz

Performance characteristics

- Frequency range: DC-50GHz
- Full positive power, with enable terminal
- Can be fully shut down
- Insertion loss : 3.0dB@50GHz
- Isolation: 42dB
- On-state VSWR : 1.3
- 50Ohm input / output
- Chip size: 1.25 x 1.1 x 0.1mm

Product Introduction

GSW-0050DT-P-PD is a GaAs MMIC single-pole double-throw transmitter switch chip with 50Ω matching at the input/output ends and a frequency range covering DC~50 GHz . The chip is powered by +5V, + 5V /0V positive level control (compatible with +3.3V), switching speed of 20ns , and 1dB compression input power of + 20dBm .

Use restriction parameter¹

Control voltage range	-0.5V ~ + 6V
Supply voltage range	+6V
Maximum input power	+27dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

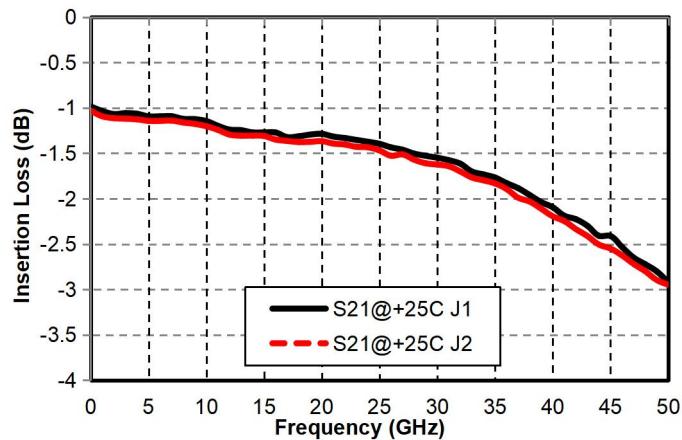
Electrical parameters (TA = +25°C , EN = 0V, VDD = +5V, VC = 0/+5V)

index	Minimum	Typical Value	Maximum	unit
Frequency Range		DC-50		GHz
Insertion loss @50GHz	-	3.0	-	dB
Isolation	-	42	-	dB
On-state input return loss	-	18	-	dB
On-state output return loss	-	18	-	dB
P-1dB	-	20	-	dBm
Switching speed	-	20	-	ns
Input high level voltage	2.7	3.3	5	V
Input low level voltage	0	-	0.8	V
Control current		1		mA
voltage		+5		V
Quiescent Current	-	1.5	-	mA

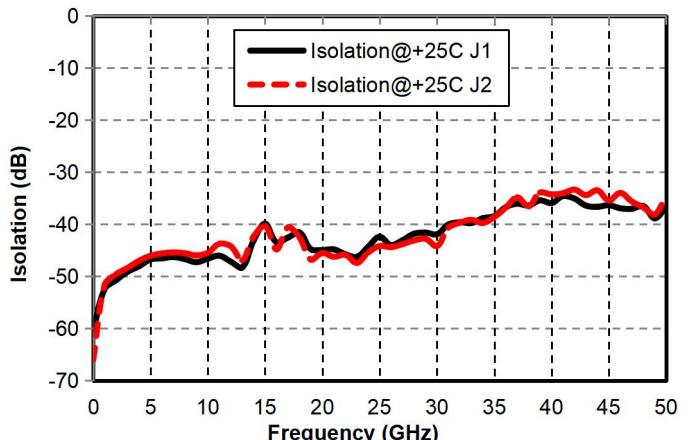
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Main index test curve

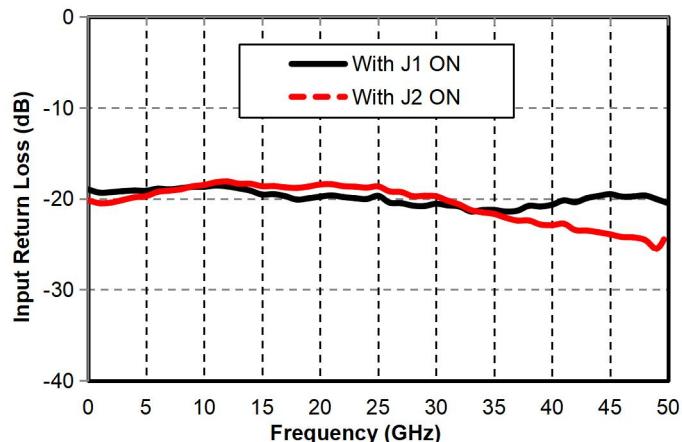
Insertion Loss vs. Operating Frequency



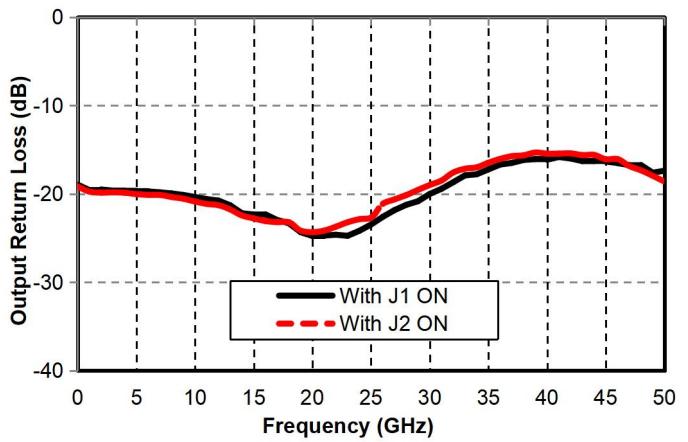
Isolation vs. Operating Frequency



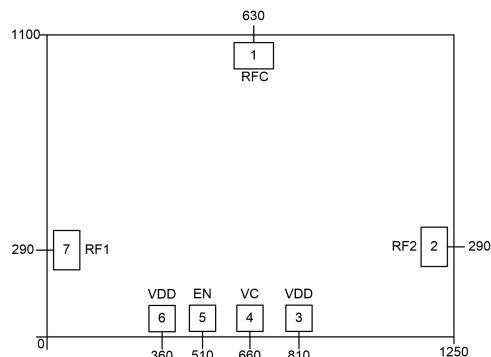
Input Return Loss vs. Operating Frequency
(On State)



Output Return Loss vs. Operating Frequency
(On State)



Appearance structure



The units in the figure are all micrometers (dimensional tolerance: ± 5 0um.)

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Bonding point definition

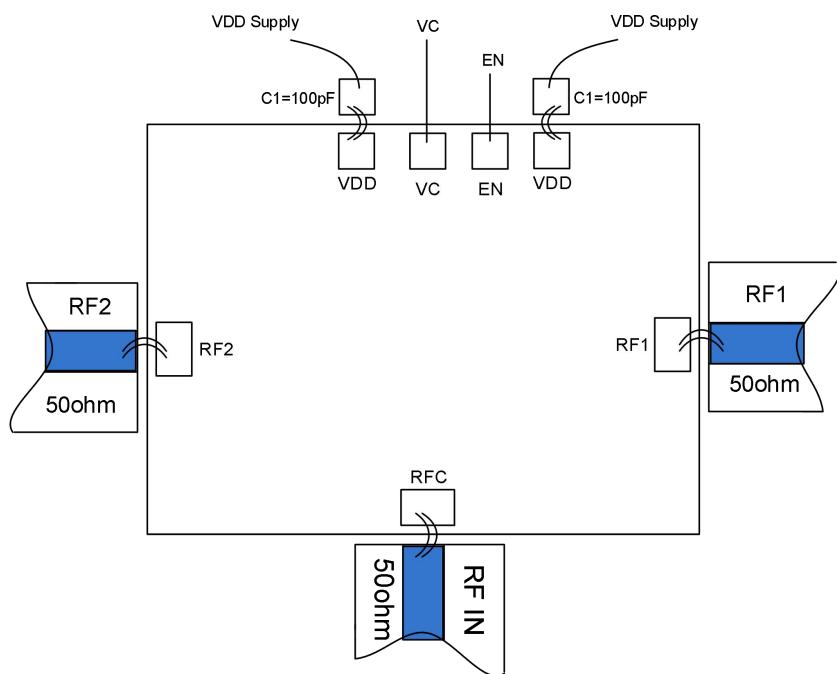
Bonding point number	Function Symbol	Functional Description
1	RFC	RF signal input and output terminals require external broadband DC blocking capacitors
2, 7	RF1/RF2	RF signal input and output terminals require external broadband DC blocking capacitors
4	VC	Positive level control port
3, 6	VDD	Power supply voltage (select one)
5	EN	Enable control port
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Truth table :

VDD	EN(V)	CTRL (V)	state
+5V	0	Low (0)	RFC-RF1
	0	High (1)	RFC-RF2 Pass
	5	-	All Off

High (1), +2.7~ +5V; Low (0), 0~ + 0.8V

Recommended assembly drawing



VDD at either end .