

## GaAs MMIC SPDT Reflective Switch Chip, DC-40GHz

### Performance characteristics

- Frequency range: DC -40GHz
- Insertion loss : 2.0 dB @ 40 GHz
- Isolation: 52dB
- On- state VSWR : 1.2
- Integrated logic control
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.6 x 1.15 x 0.1mm

### Product Introduction

GSW-0040DT-N-PD is a GaAs MMIC single-pole double-throw reflective switch chip with 50Ω matching at the input/output ends and a frequency range of DC ~40 GHz . The chip is powered by -5V, 0V / +5V positive level control (compatible with +3.3V), switching speed of 30ns , P - 1dB input power of + 21dBm .

Use restriction parameter <sup>1</sup>	
Control voltage range	-0.5V ~ + 6V
Supply voltage range	- 6V
Maximum input power	+25dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

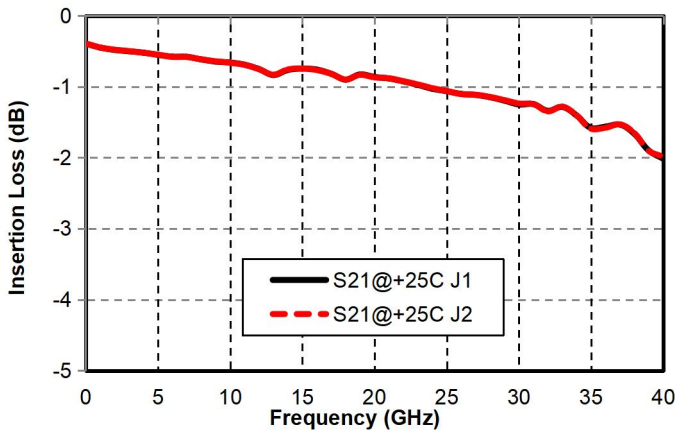
【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters ( TA = +25°C , VEE = -5V )				
index	Minimum	Typical Value	Maximum	unit
Frequency Range	DC-40			GHz
Insertion loss @40GHz	-	2.0	-	dB
Isolation	-	52	-	dB
On-state input return loss	-	23	-	dB
On-state output return loss	-	23	-	dB
P-1dB	-	21	-	dBm
IIP3	-	37	-	dBm
Switching speed	-	30	-	ns
Control voltage	-	0/+5	-	V
Control current	-	600	-	uA
voltage	-	-5	-	V
Quiescent Current	-	1.5	-	mA

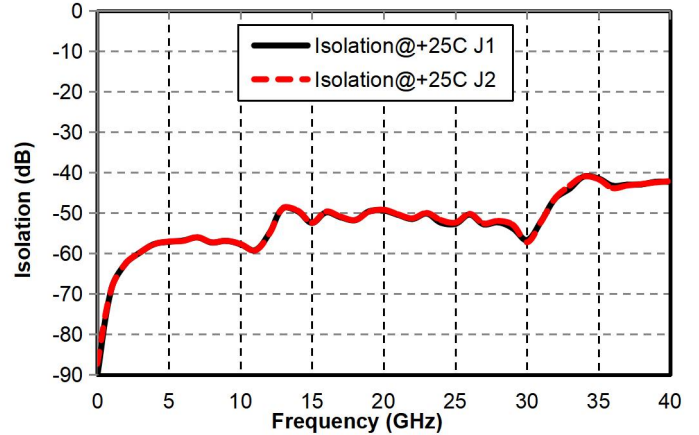
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Main index test curve

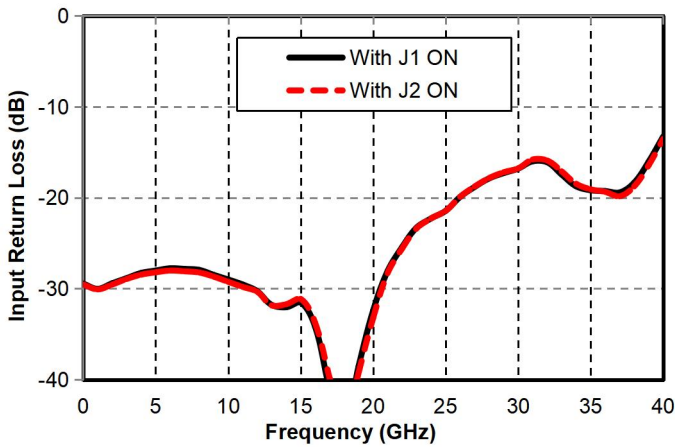
Insertion Loss vs. Operating Frequency



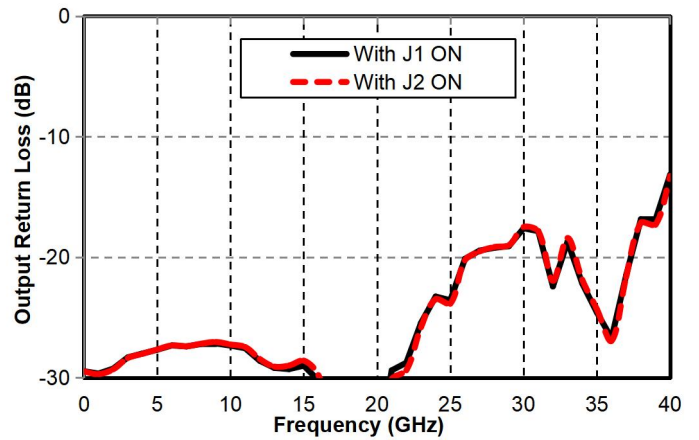
Isolation vs. Operating Frequency



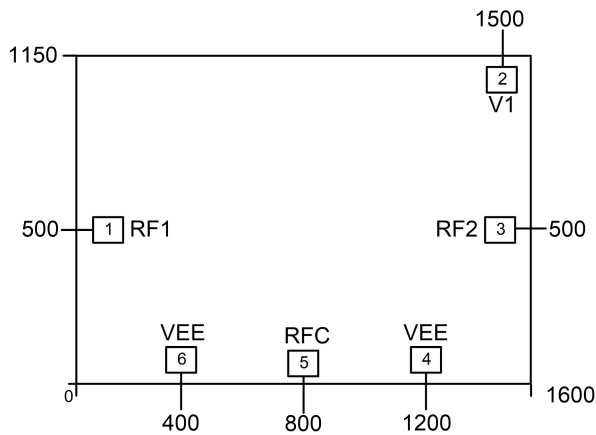
Input Return Loss vs. Operating Frequency  
( On State )



Output Return Loss vs. Operating Frequency  
( On State )



Appearance structure <sup>2</sup>



【2】 The units in the figure are all micrometers (dimensional tolerance:  $\pm 5.0\mu\text{m}$ .)

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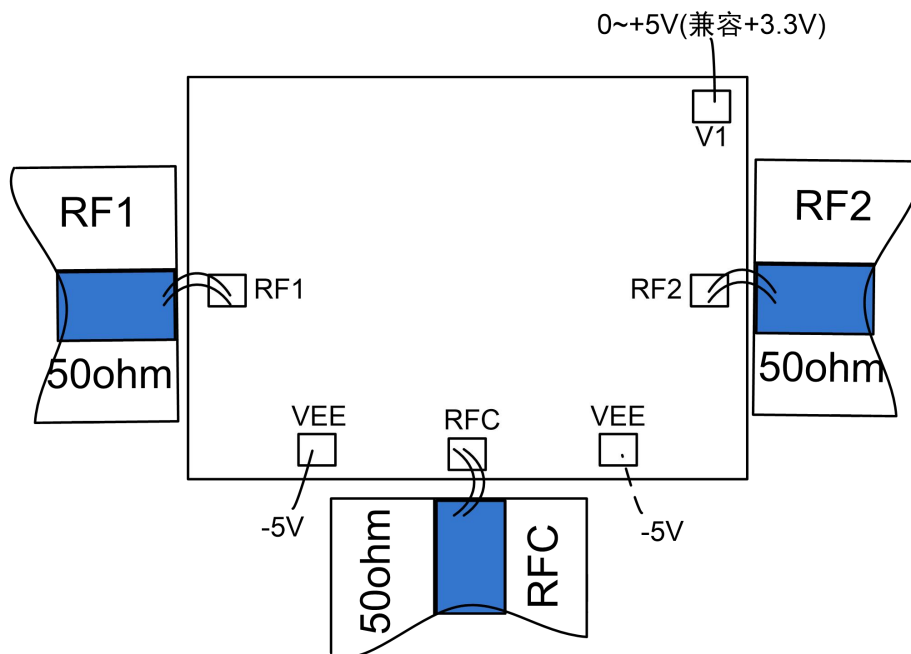
Bonding point definition		
Bonding point number	Function Symbol	Functional Description
5	RF COMM	RF signal input terminal , no internal DC blocking capacitor
1,3	RF OUTPUT	RF signal output terminal , no internal DC blocking capacitor
2	VC	Control Port
4, 6	VEE*	voltage
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

\* Just connect to VEE on either side.

### Truth table :

VEE	IEE	VC	state
-5V	1.5mA	0V	Shutdown
		+5V ( compatible with +3.3V)	Conductivity

### Recommended assembly drawing



VEE port can be connected in parallel with a bypass capacitor > 100nF