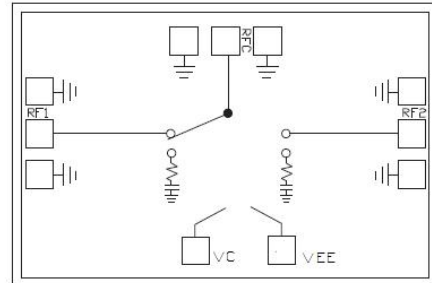


## GaAs MMIC SPDT Switch Chip, DC-40GHz

### Performance characteristics

- Frequency range: DC - 40 GHz
- Insertion loss : 2.0 dB @ 40 GHz
- Isolation: 52dB
- On-state VSWR : 1.2
- Integrated logic control
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.72 x 1.71 x 0.1mm

### Block Diagram



### Product Introduction

GSW-0040BDT-PDM is a GaAs MMIC single-pole double-throw switch chip with 50Ω matching at the input/output ends, a frequency range covering DC ~ 40 GHz , a -5V power supply, 0 V / +5V positive level control , a switching speed of 30 ns, and a P- 1dB input power of +2 1 dBm . GSW-0040BDT-PDM and GSW-0040BDT-PD are mirror versions of each other.

#### Use restriction parameter <sup>1</sup>

Control voltage range	-0.5V ~ + 6V
Supply voltage range	- 6V
Maximum input power	+25dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

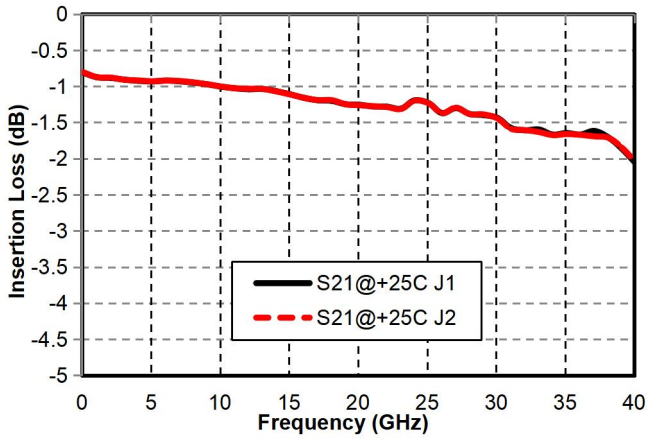
#### Electrical performance parameters ( TA = +25°C , VEE = -5V )

index	Minimum	Typical Value	Maximum	unit
Frequency Range	DC-40			G Hz
Insertion loss @40GHz	-	2.0	-	dB
Isolation	-	52	-	dB
On-state input return loss	-	twenty three	-	dB
On-state output return loss	-	twenty three	-	dB
P-1dB	-	twenty one	-	dBm
IIP3	-	37	-	dBm
Switching speed	-	30	-	ns
Control voltage	-	0/+5	-	V
Control current	-	600	-	uA
voltage	-	-5	-	V
Quiescent Current	-	3	-	mA

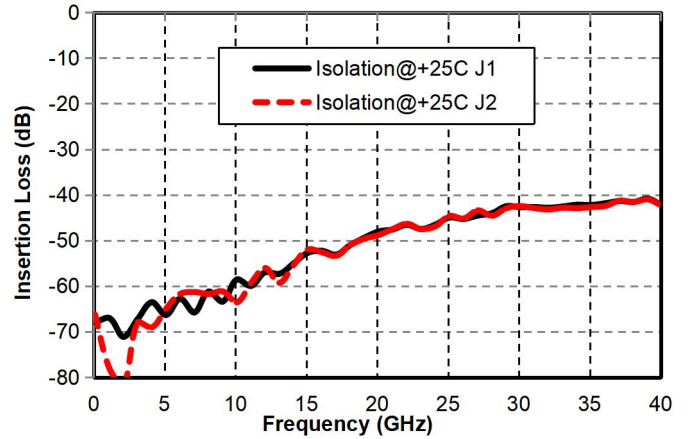
## GaAs MMIC SPDT Switch Chip, DC-40GHz

### Main index test curve

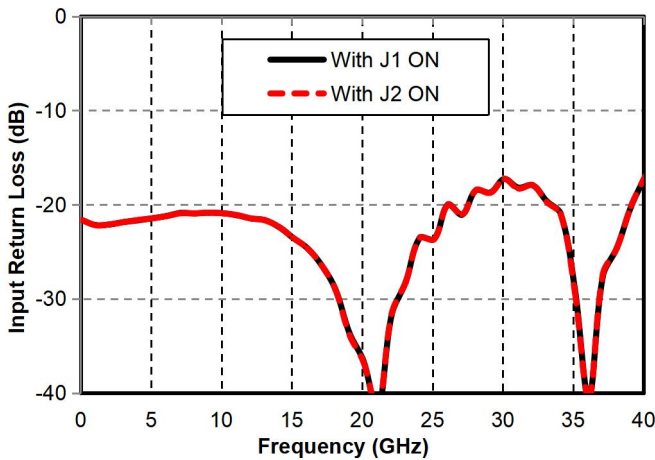
Insertion Loss vs. Operating Frequency



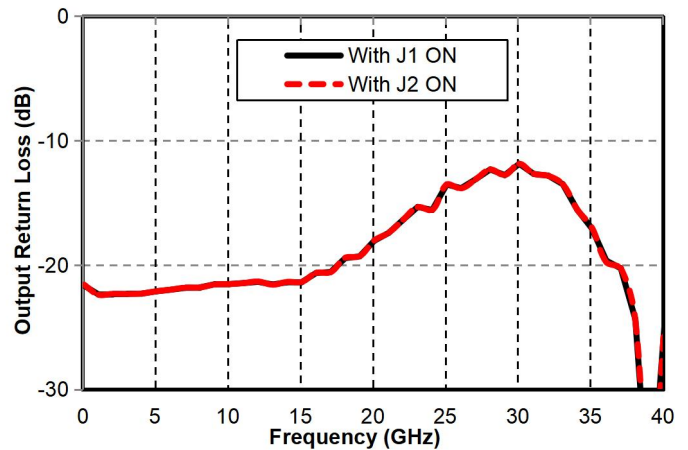
Isolation vs. Operating Frequency



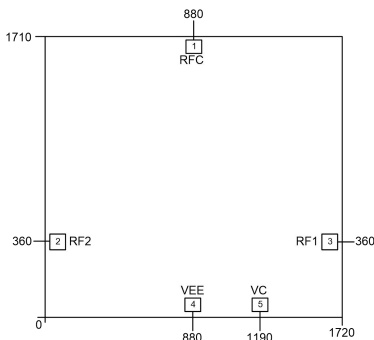
Input Return Loss vs. Operating Frequency (On State)



Output Return Loss vs. Operating Frequency (On State)



### Appearance structure <sup>2</sup>



**[2]** The units in the figure are all micrometers (dimensional tolerance:  $\pm 5.0\mu\text{m}$ .)

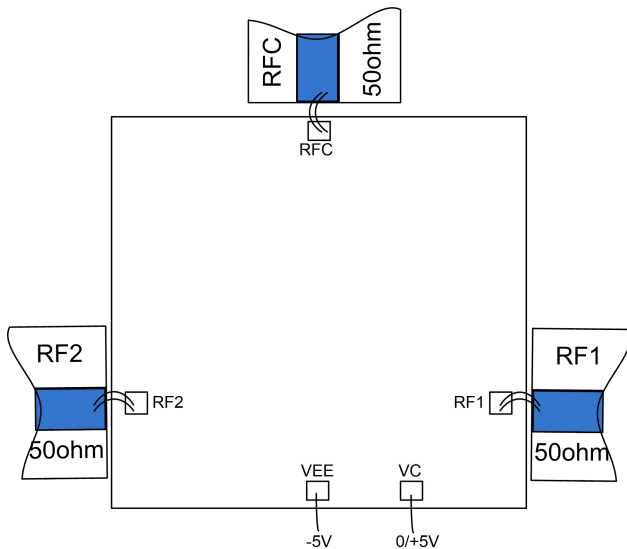
## GaAs MMIC SPDT Switch Chip, DC-40GHz

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF COMM	RF signal input terminal , no internal DC blocking capacitor
2,3	RF OUTPUT	RF signal output terminal , no internal DC blocking capacitor
4	VEE	voltage
5	VC	Level control port
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

### Truth table

VEE	VC	Conductivity
-5V	+5V	RF1
-5V	0V	RF2

### Recommended assembly drawing



VEE port can be connected in parallel with a bypass capacitor > 100nF