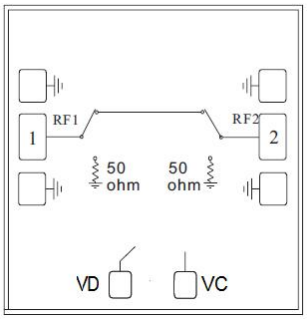
GSW - 0020ST-P-PD

GaAs MMIC SPST Absorptive Switch Chip, DC -20GHz

Performance characteristics

- Frequency range: DC -20GHz
- Insertion loss : 1.1 dB @ 18 GHz
- Isolation: 57dB
- On-state VSWR : 1. 2
- Integrated logic control (all positive)
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.25 x 1.10 x 0.1mm

Block Diagram



Product Introduction

GSW-0020ST-P-PD is a GaAs MMIC single-pole single-throw absorptive switch chip with 50Ω matching at the input/output ends and a frequency range covering DC~20 GHz . The chip is powered by +5V, 0V / +5V (compatible with +3.3V) positive level control , switching speed of 20ns , P -1dB input power of + 26dBm .

Use restriction parameter [1]	
Control voltage range	-0.5V ～ + 6V
Supply voltage range	+6V
Maximum input power	+30dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , VDD = +5V, VC = 0/+5V)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range		DC-20		G Hz
Insertion loss @18GHz	-	1.1	-	dB
Isolation	-	57	-	dB
On-state input return loss	-	25	-	dB
On-state output return loss	-	25	-	dB
P-1dB @ ＞1GHz	-	26	-	dBm
Switching speed	-	20	-	ns
Control high level	3	3.3	5	V
Control low level	0	-	0.8	V
Control current		600		uA
voltage	-	+5	-	V
Quiescent Current	-	1.5	-	mA

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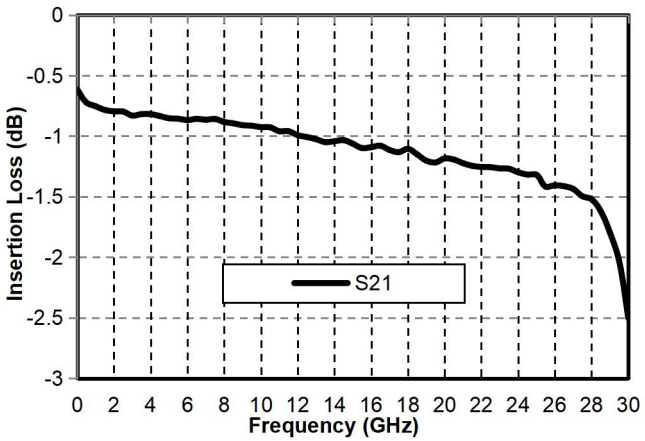
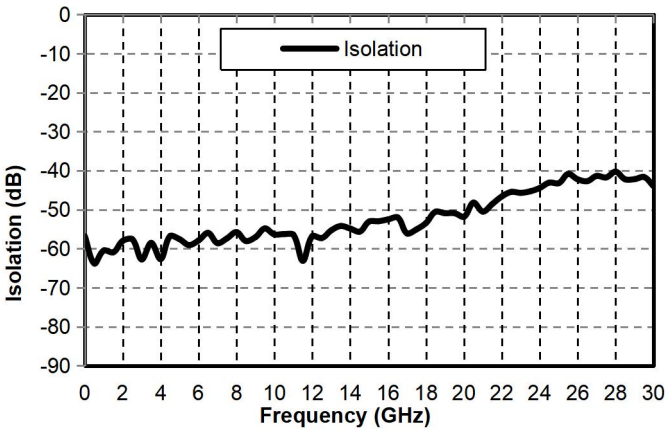
Main index test curve

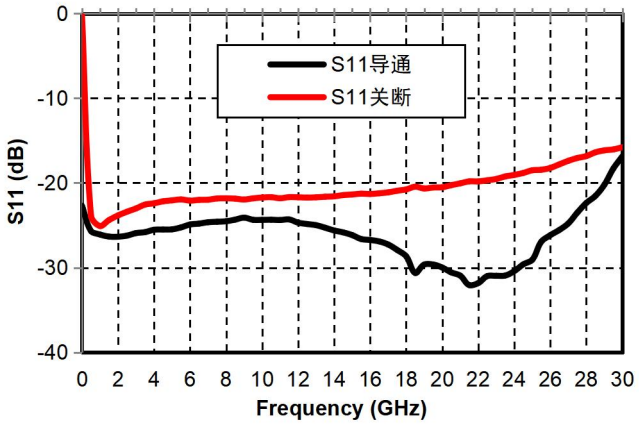
Insertion Loss vs. Operating Frequency



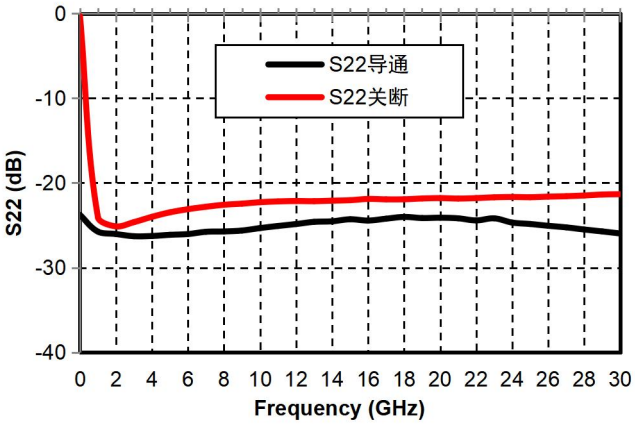
Isolation vs. Operating Frequency



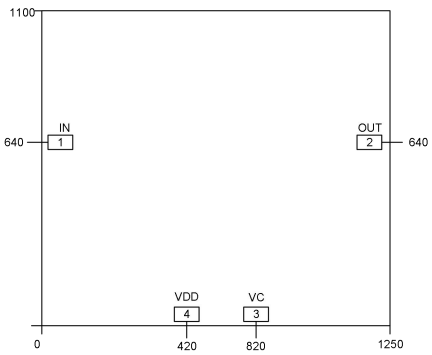
Input Return Loss vs. Operating Frequency (On/Off)



Output Return Loss vs. Operating Frequency (On/Off)



Appearance structure [2]



【2】The units in the figure are all micrometers (dimensional tolerance: ± 5 0um.)

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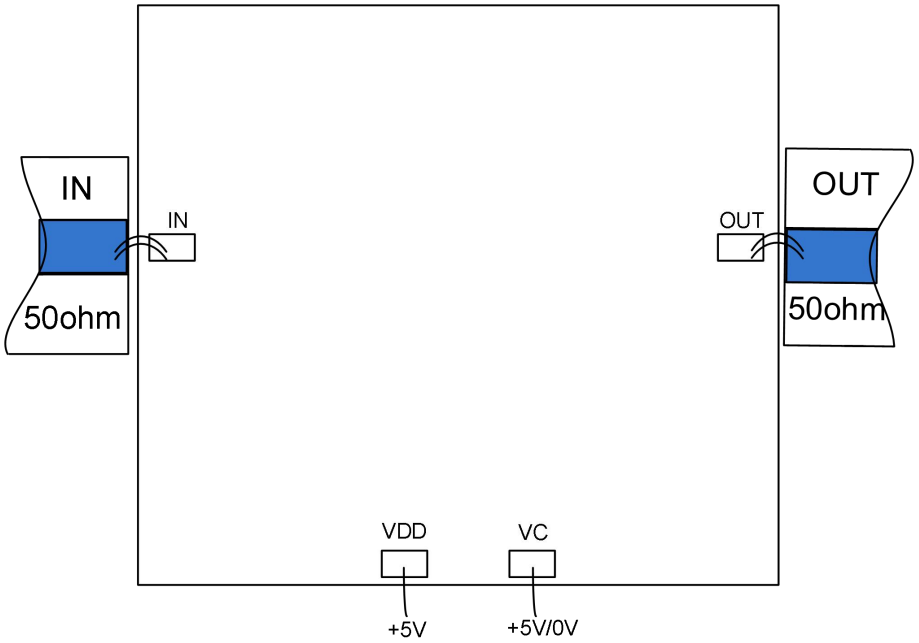
Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	IN	RF signal input and output terminals , no internal DC blocking capacitors
2	OUT	RF signal input and output terminals , no internal DC blocking capacitors
3	VC	Positive level control port
4	VDD	voltage
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Truth table

VDD	VC	path
+ 5V	+ 5V /+3.3V	Continuity
+ 5V	0V	Shutdown

Recommended assembly drawing



The VDD port can be connected in parallel with a bypass capacitor > 100nF

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