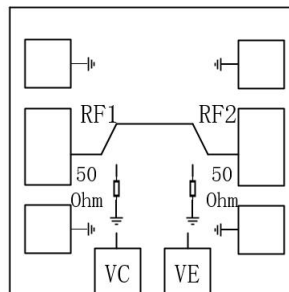


## GaAs MMIC SPST Absorptive Switch Chip, DC-20GHz

### Performance characteristics

- Frequency range: DC- 20GHz
- Insertion loss : 1.2dB@ 20GHz
- Isolation: 46dB
- On/off standing wave: 1. 2
- Integrated logic control
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.1 x 1.1 x 0.1mm

### Block Diagram



### Product Introduction

GSW-0020ST-N-PD is a GaAs MMIC single-pole single-throw absorptive switch chip with 50Ω matching at the input/output ends and a frequency range covering DC ~20 GHz . The chip is powered by -5V, 0V / +5V positive level control , switching speed of 30ns, and P -1dB input power of +25dBm .

#### Use restriction parameter <sup>1</sup>

Control voltage range	-0.5V ~ + 6V
Supply voltage range	- 6V
Maximum input power	+30dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

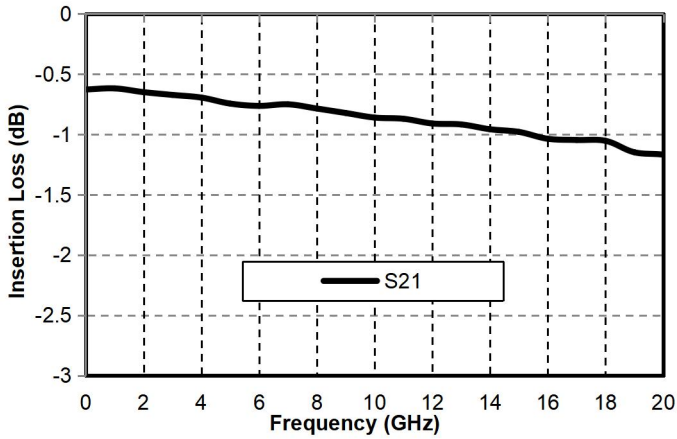
#### Electrical performance parameters ( TA = +25°C , VE = -5V, VC = 0/+5V )

index	Minimum	Typical Value	Maximum	unit
Frequency Range	DC-20			GHz
Insertion loss @20GHz	-	1.2	-	dB
Isolation	-	46	-	dB
On-state input return loss	-	22	-	dB
On-state output return loss	-	22	-	dB
P-1dB @0.5-20 GHz	-	25	-	dBm
Switching speed	-	30	-	ns
Control voltage	-	0/+5	-	V
Control current	-	1	-	mA
voltage	-	-5	-	V
Quiescent Current	-	2	-	mA

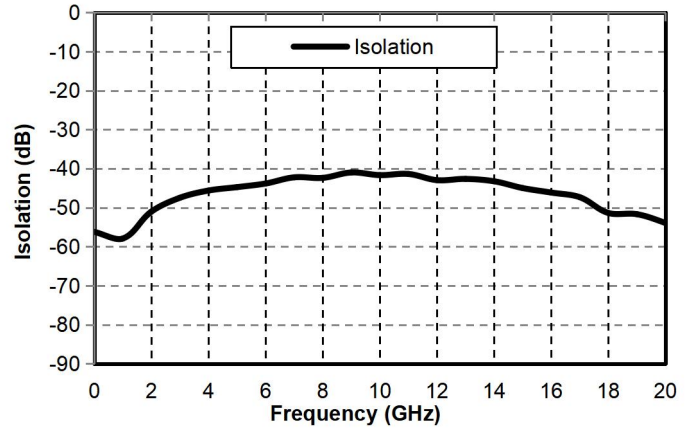
## GaAs MMIC SPST absorptive switch chip, DC- 20 GHz

Main index test curve

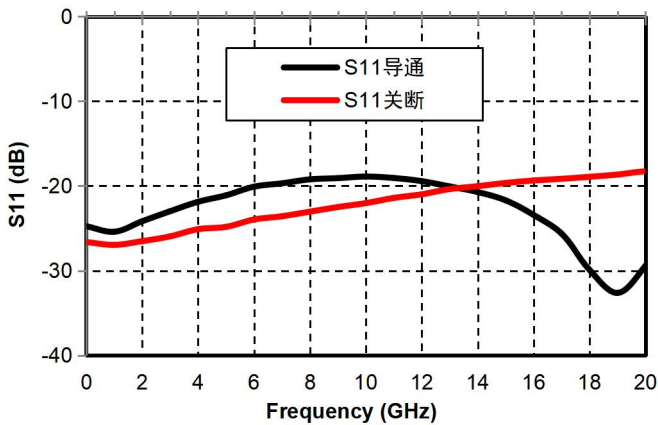
Insertion Loss vs. Operating Frequency



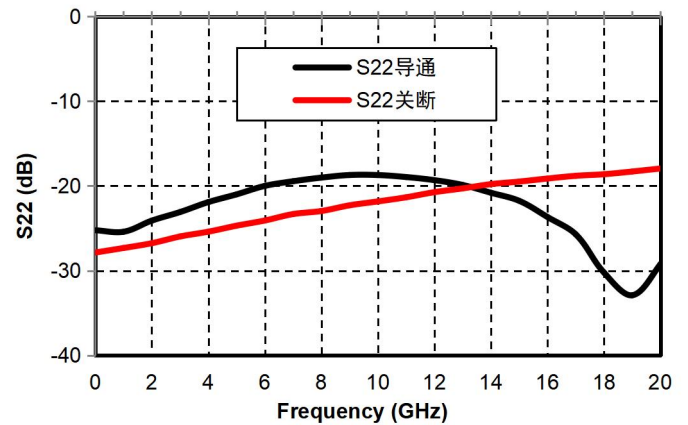
Isolation vs. Operating Frequency



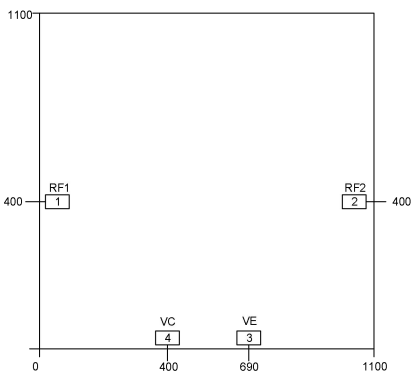
Input Return Loss vs. Operating Frequency  
( On/Off )



Output Return Loss vs. Operating Frequency  
( On/Off )



Appearance structure <sup>2</sup>



**[2]** The units in the figure are all micrometers (dimensional tolerance:  $\pm 5.0\mu\text{m}$ .)

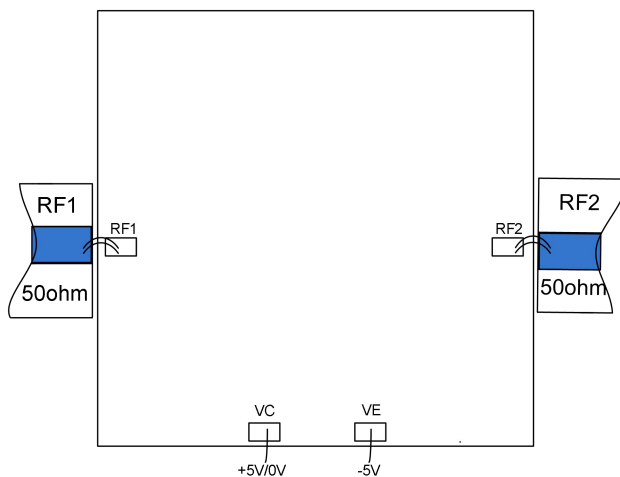
## GaAs MMIC SPST absorptive switch chip, DC- 20 GHz

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF 1	RF signal input / output terminal , no internal DC blocking capacitor
2	RF2	RF signal input / output terminal , no internal DC blocking capacitor
3	VC	Positive level control port
4	VE	voltage
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

### Truth table :

V E	VC	path
- 5V	+ 5V	Continuity
- 5V	0V	Shutdown

### Recommended assembly drawing



VE port can be connected in parallel with bypass capacitor > 100nF