

GaAs MMIC Reflective SPDT Switch Chip, DC-20GHz

Performance characteristics

- Frequency range: DC -20GHz
- Insertion loss : 1.2 dB @ 20 GHz
- Isolation: 46dB
- On-state VSWR: 1.2
- Integrated control logic
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.25 x 1.1 x 0.1mm

Product Introduction

GSW-0020DT-N-PD is a GaAs MMIC reflective single-pole double-throw switch chip with 50Ω matching at the input/output end and a frequency range covering DC ~20GHz , the chip adopts -5V power supply, 0V / +5V positive level control , switching speed 30ns , P - 1dB input power + 23dBm .

Use restriction parameter ¹	
Control voltage range	-0.5V ~ + 6V
Supply voltage range	- 6V
Maximum input power	+30dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

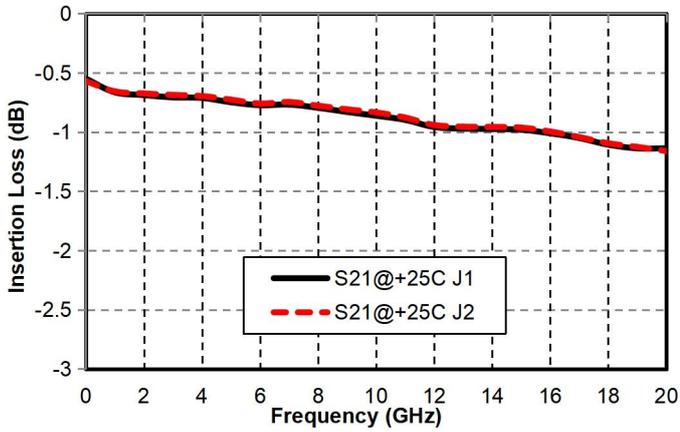
【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , VEE = -5V , VC = 0V/+5V)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range	DC-20			GHz
Insertion loss @21GHz	-	1.2	-	dB
Isolation	-	46	-	dB
On-state input return loss	-	19	-	dB
On-state output return loss	-	20	-	dB
P-1dB	-	23	-	dBm
Switching speed	-	30	-	ns
Control voltage	-	0/+5	-	V
Control current	-	500	-	uA
voltage	-	-5	-	V
Quiescent Current	-	3	-	mA

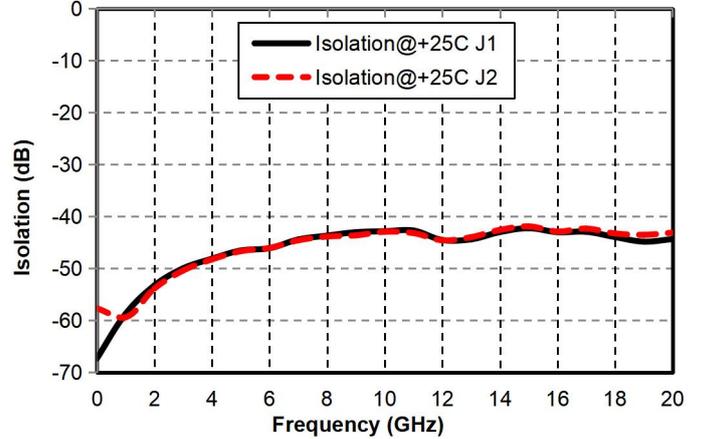
GaAs MMIC Absorptive SPDT Switch Chip, DC- 200 GHz

Main index test curve

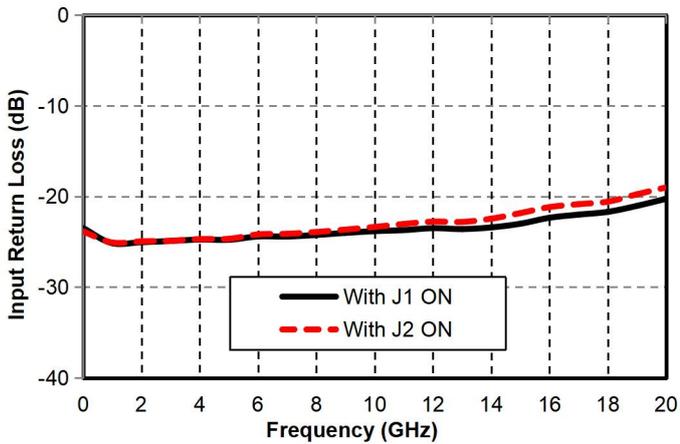
Insertion Loss vs. Operating Frequency



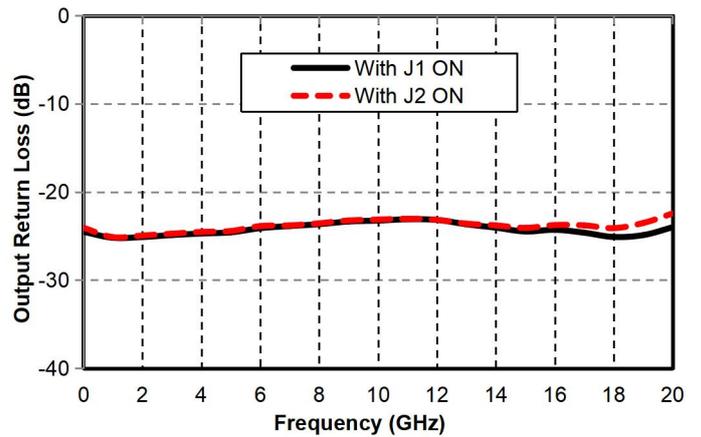
Isolation vs. Operating Frequency



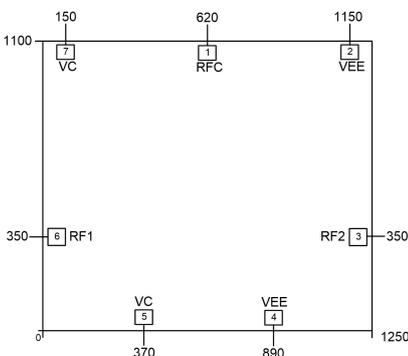
Input Return Loss vs. Operating Frequency
(On State)



Output Return Loss vs. Operating Frequency
(On State)



Appearance structure ²



【 2 】 All units in the figure are micrometers

GaAs MMIC Absorptive SPDT Switch Chip, DC-20GHz

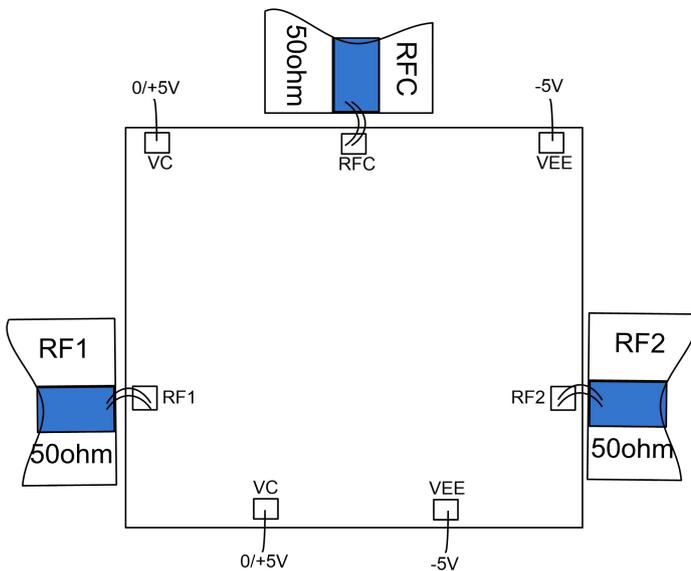
Bonding point definition

Bonding point number	Function Symbol	Functional Description
1	RF COMM	RF signal input terminal , no internal DC blocking capacitor
2,3	RF OUTPUT	RF signal output terminal , no internal DC blocking capacitor
4	VC	Positive level control port
5	VEE	Power supply voltage (used for positive level control)
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Truth table

VEE	VC	path
-5V	5V	RFC-RF1
-5V	0V	RFC-RF2

Recommended assembly drawing



connect VEE and VC on either side .