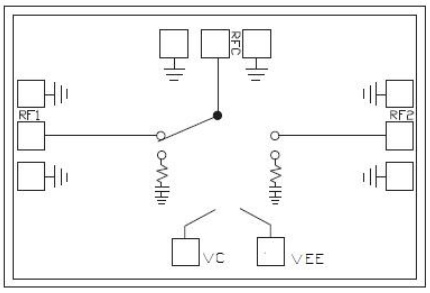
GSW-0019DT-PDM

GaAs MMIC SPDT absorptive switch chip, DC- 19GHz

Performance characteristics

- Frequency range: DC - 19 GHz
- Insertion loss : 1.4 dB @ 20 GHz
- Isolation: 56dB
- On-state VSWR : 1. 2
- Integrated logic control
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.72 x 1.19 x 0.1mm

Block Diagram



Product Introduction

GSW-0019DT-PDM is a GaAs MMIC single-pole double-throw absorptive switch chip with 50Ω matching at the input/output ends, a frequency range covering DC ~ 19 GHz , a -5V power supply, 0 V / +5V positive level control (compatible with +3.3 V), a switching speed of 30 ns, and a P- 1 dB input power of +23 dBm . GSW -0019DT-PDM and GSW-0019DT-PD are mirror versions of each other.

Use restriction parameter [1]	
Control voltage range	-0.5V ～ + 6V
Supply voltage range	- 6V
Maximum input power	+30dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , VEE = -5V)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range		DC -19		GHz
Insertion loss @20GHz	-	1.4	-	dB
Isolation	-	56	-	dB
On-state input /output return loss	-	19	-	dB
Off-state output return loss	-	20	-	dB
P-1dB @0.5~20 GHz	-	22	-	dBm
Switching speed	-	30	-	ns
Control high level	+3	+3.3 V	+5	V
Control low level	0	-	+0.8	V
Control current	-	600	-	uA
voltage	-	-5	-	V
Quiescent Current	-	3	-	mA

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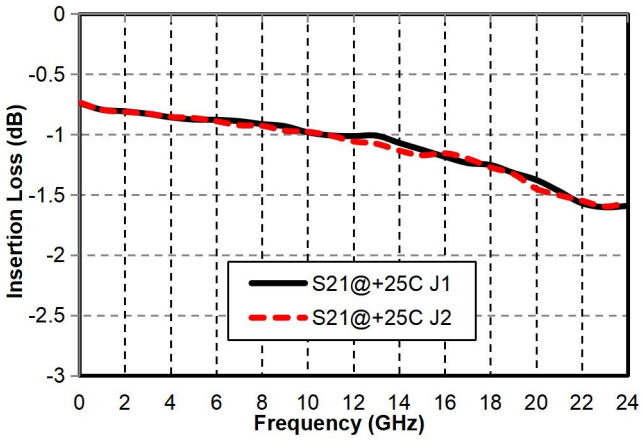
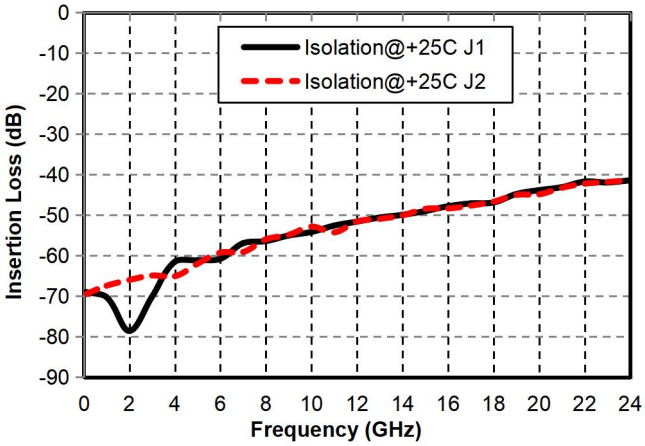
Main index test curve

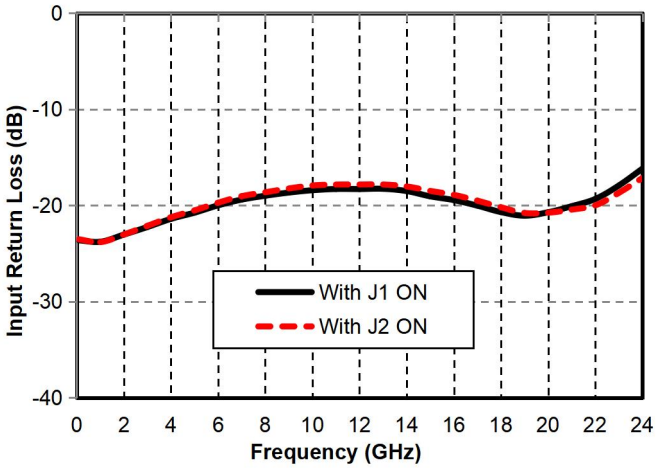
Insertion Loss vs. Operating Frequency



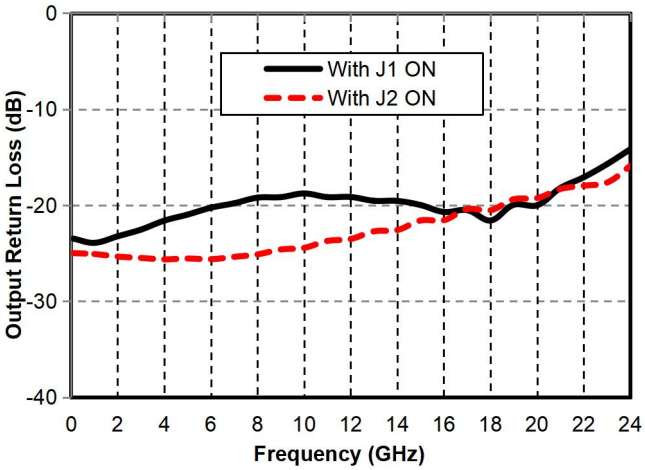
Isolation vs. Operating Frequency



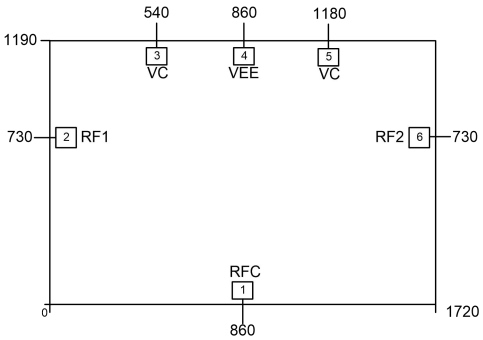
Input Return Loss vs. Operating Frequency (On State)



Output Return Loss vs. Operating Frequency (On State)



Appearance structure [2]



【2】The units in the figure are all micrometers (dimensional tolerance: ± 5 0um.)

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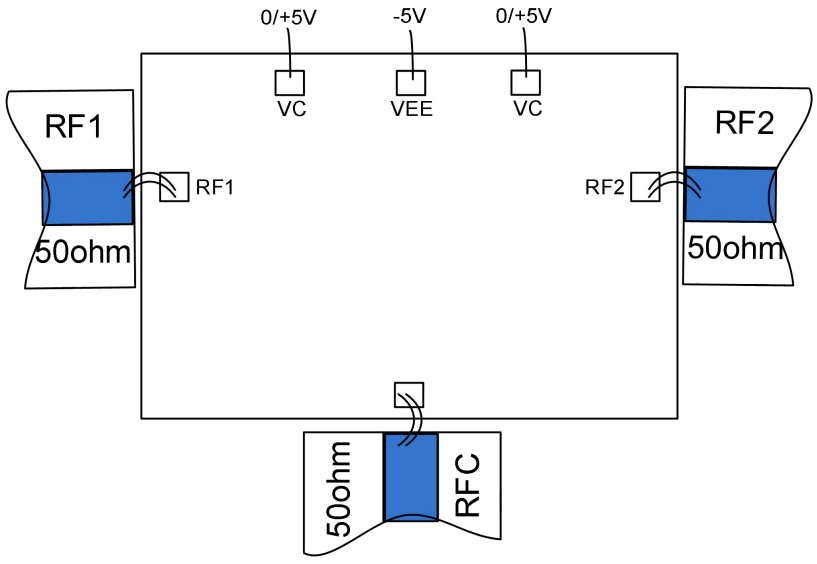
Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF COMM	RF signal input terminal , no internal DC blocking capacitor
2, 6	RF1, RF2	RF signal output terminal , no internal DC blocking capacitor
3, 5	VC	Positive level control port (connect to VC on either side)
4	VEE	voltage
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Truth table :

VEE	VC	path
-5V	5V (compatible with 3.3V)	RFC-RF1
-5V	0V	RFC-RF2

Recommended assembly drawing



VEE port can be connected in parallel with a bypass capacitor > 100nF