

GaAs MMIC SPDT absorptive switch chip , DC -12G

Performance characteristics

- Frequency range: DC~ 12GHz
- Insertion loss : 1.4 dB @ 12 GHz
- Isolation: 55dB
- On-state VSWR : 1.2
- Off-state standing wave ratio: 1.5
- Integrated logic control (all positive)
- Can be fully shut down
- 50Ohm input / output
- Chip size: 1.25 x 1.1 x 0.1mm

Product Introduction

GSW-0012DT-P-PD is a GaAs MMIC single-pole double-throw absorptive switch chip with 50Ω matching at the input/output end and a frequency range covering DC~ 12 GHz , the chip adopts +5V power supply, +5V /0V positive level control (compatible with +3.3V), switching speed 15ns, P - 1dB input power + 24dBm .

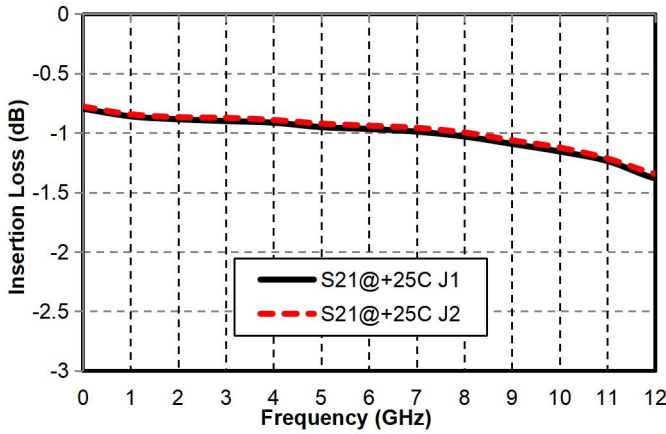
Use restriction parameter ¹	
Control voltage range	-0.5V ~ +6V
Supply voltage range	+6V
Maximum input power	+27dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

Electrical parameters (TA = +25°C , EN = 0V, VDD = +5V, CTRL = 0/+5V)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range	DC-12			G Hz
Insertion loss @10GHz	-	1.2	-	dB
Isolation	-	55	-	dB
On-state input/output return loss	-	20	-	dB
Off-state output return loss	-	16	-	dB
P-1dB@1~10G	-	24	-	dBm
Switching speed	-	15	-	ns
Input high level	2.7	-	5	V
Input low level	0	-	0.8	V
Control current		-	1	mA
voltage		+5		V
Quiescent Current	-	1.5	-	mA

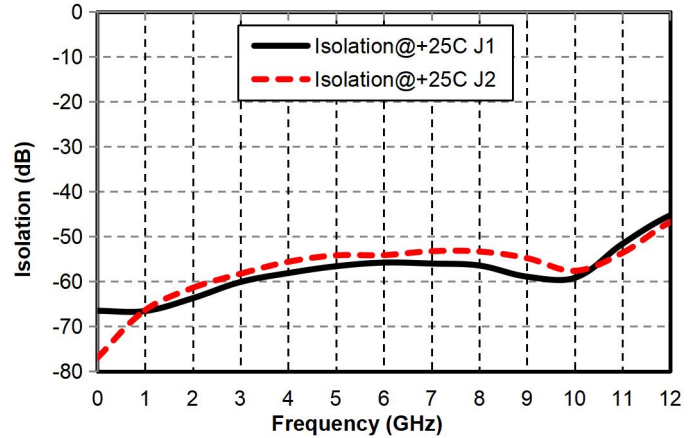
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Main index test curve

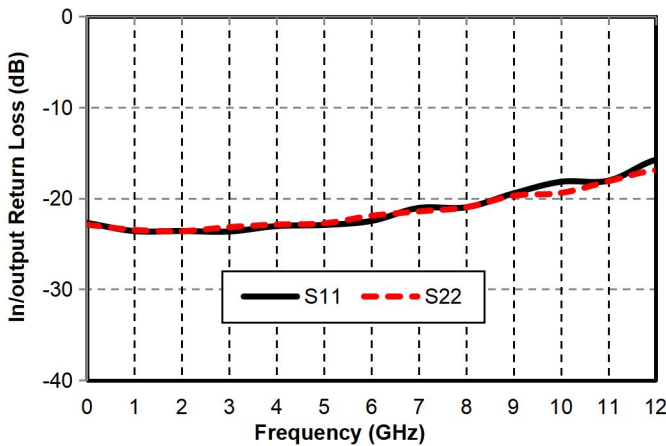
Insertion Loss vs. Operating Frequency



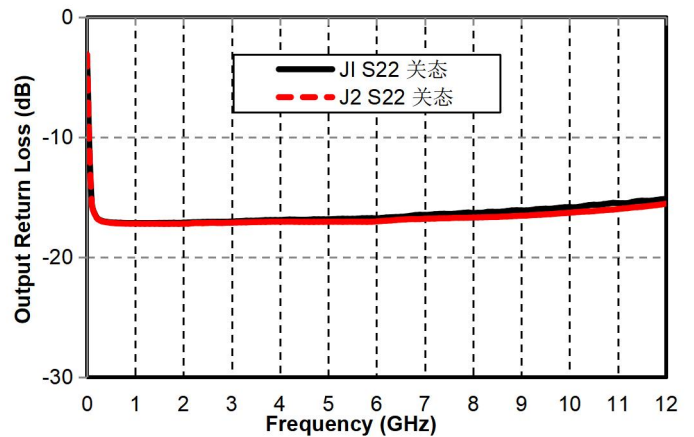
Isolation vs. Operating Frequency



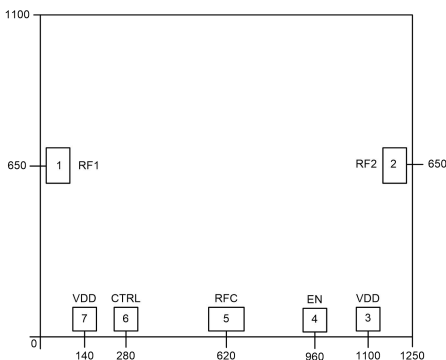
Input /Output Return Loss vs. Operating Frequency (On State)



Output Return Loss vs. Operating Frequency (Off State)



Appearance structure



The units in the figure are all micrometers (dimensional tolerance: $\pm 5.0\mu\text{m}$)

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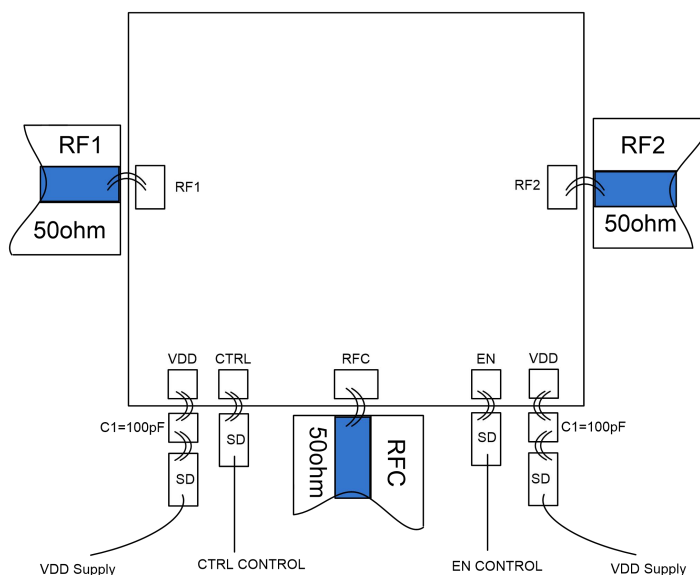
Bonding point definition		
Bonding point number	Function Symbol	Functional Description
5	RFC	RF signal input terminal , requires external broadband DC blocking capacitor
1, 2	RF1, RF2	RF signal output terminal requires external broadband DC blocking capacitor
3, 7	VDD	voltage
4	EN	Enable control terminal
6	CTRL	Positive level control port
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Truth Table

VDD	EN	CTRL	Function
+5V	0	Low (0)	RFC-RF1
	0	High (1)	RFC-RF2
	+5	-	All Off

High (1), +2.7~ +5V; Low (0), 0~ + 0.8V

Recommended assembly drawing



The VDD port can be connected in parallel with a bypass capacitor > 100nF