GSW-0006DT-N-PD

GaAs MMIC SPDT reflective switch chip, DC-6GHz

Performance characteristics

- Frequency range: DC -6GHz
- Insertion loss : 0.3dB typ.
- Isolation: 50dB typ.
- On- state VSWR : 1.3
- Integrated logic control
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 0.83 x 0.88 x 0.1mm

Product Introduction

GSW-0006DT-N-PD is a GaAs MMIC single-pole double-throw reflective switch chip with 50Ω matching at the input/output ends and a frequency range covering DC ~6 GHz . The chip is powered by -5V, 0V / +5V (compatible with +3.3V) positive level control , switching speed of 20ns, and 1dB compression input power of + 30dBm .

Use restriction parameter [1]	
Control voltage range	-0.5V ～ + 6V
Supply voltage range	-6V
Maximum input power	+3 3 dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , VEE = -5V, VC = 0/+5V)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range		DC-6		G Hz
Insertion loss	-	0.3	-	dB
Isolation	-	50	-	dB
On-state input return loss	-	20	-	dB
On-state output return loss	-	20	-	dB
P-1dB@0.8-4GHz	-	30	-	dBm
Switching speed	-	20	-	ns
Control high level	3	3.3	5	V
Control low level	0	-	0.8	V
Control current		-	1	m A
voltage	-	-5	-	V
Quiescent Current	-	2	-	mA

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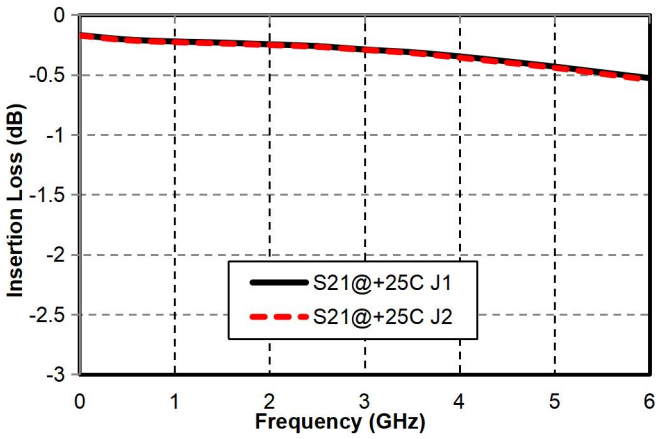
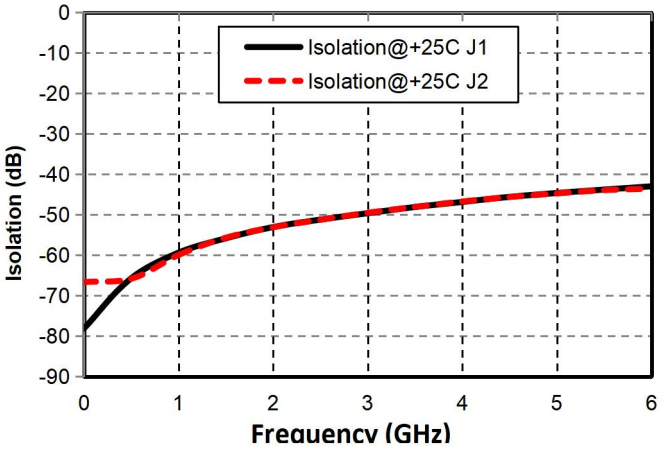
Main index test curve

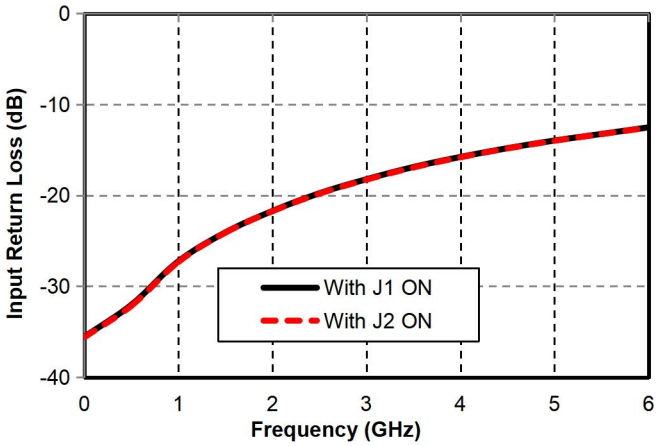
Insertion Loss vs. Operating Frequency



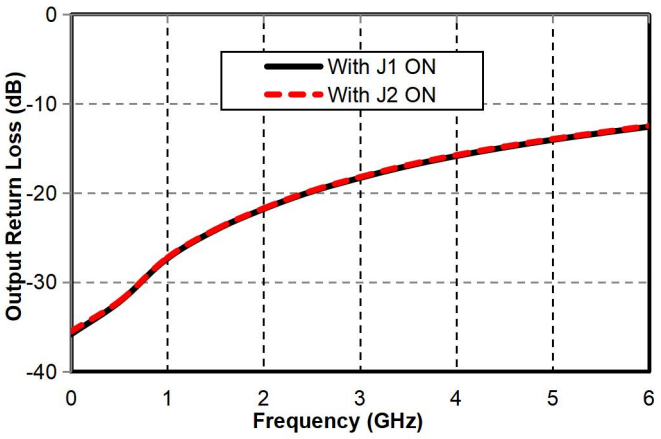
Isolation vs. Operating Frequency



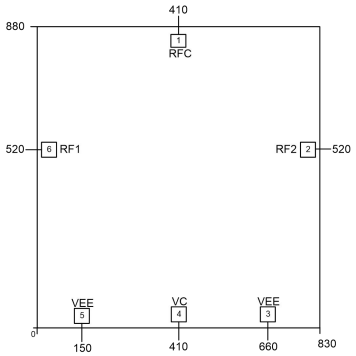
Input Return Loss vs. Operating Frequency (On State)



Output Return Loss vs. Operating Frequency (On State)



Appearance structure [2]



【2】The units in the figure are all micrometers (dimensional tolerance: ± 5 0um.)

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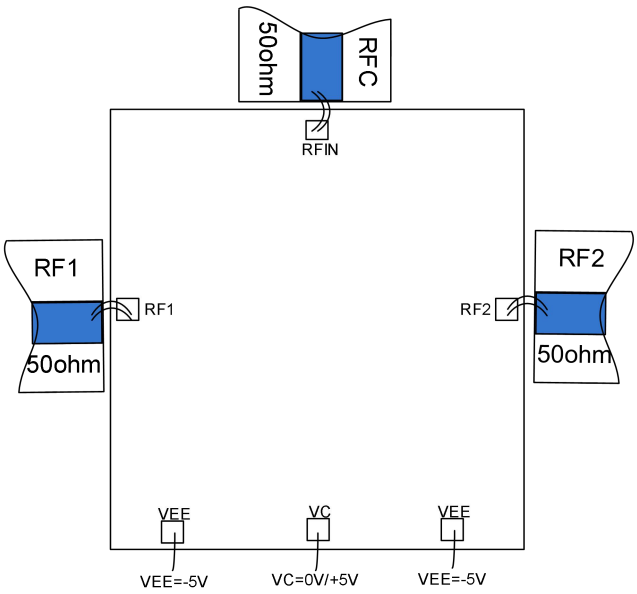
Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RFIN	RF signal input terminal , no DC blocking capacitor inside , external DC blocking capacitor is required
2, 6	RF1/RF2	RF signal output terminal , no DC blocking capacitor inside , external DC blocking capacitor is required
3, 5	VEE	voltage
4	VC	Positive level control port
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Truth table :

VEE	VC	path
-5 V	+ 5V /(compatible with +3.3V)	RF IN -RF 2
-5 V	0V	RF IN -RF 1

Recommended assembly drawing



VEE port can be connected in parallel with a bypass capacitor > 100nF .