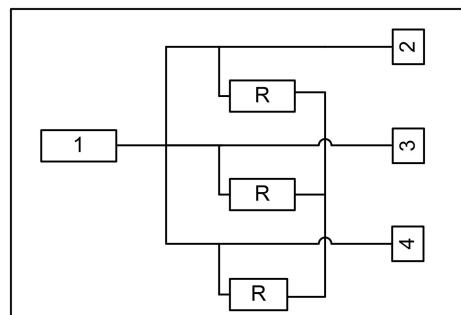


GaAs MMI C Monolithic Integrated 3-way 0-degree Power Divider, 8-12GHz

Performance characteristics

- Frequency range: 8 -12 GHz
- Insertion loss : 0.3 dB
- 50Ohm input / output
- 100% on-wafer testing
- Chip size: 1.75 x 1.2 x 0.1mm

Functional Block Diagram



Product Introduction

The GPD-08123 monolithic integrated 3-way 0- degree power divider has low insertion loss and excellent port standing wave characteristics in the frequency range of 8~12GHz , with an isolation of 29dB , and is very suitable for microwave hybrid integrated circuits and multi-chip modules. The chip uses on-chip through-hole metallization technology to ensure good grounding, does not require additional grounding measures, and is simple and convenient to use.

Use restriction parameter ¹

Maximum input power	+40dBm
Operating temperature	-55 ~ +85°C
storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

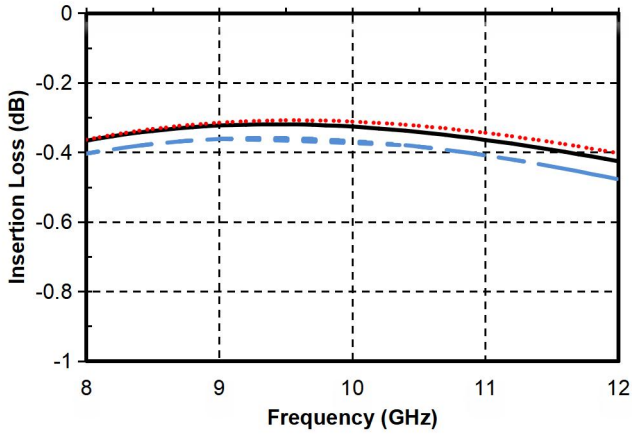
Electrical performance parameters (TA = +25°C)

index	Minimum	Typical Value	Maximum	unit
Frequency Range	8-12			GHz
Insertion loss	0.2	0.3	0.4	dB
Insertion loss fluctuation		± 0.1		dB
Isolation	23	29	-	dB
Input return loss	17	22	-	dB
Output return loss	21	25	-	dB

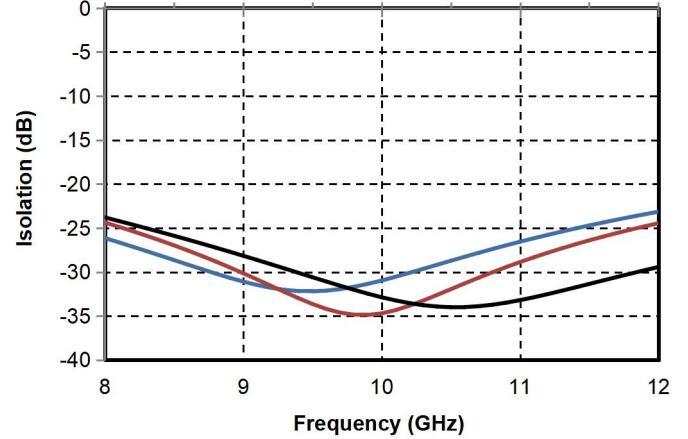
GaAs MMI C Monolithic Integrated 3-way 0-degree Power Divider, 8-12GHz

Main index test curve

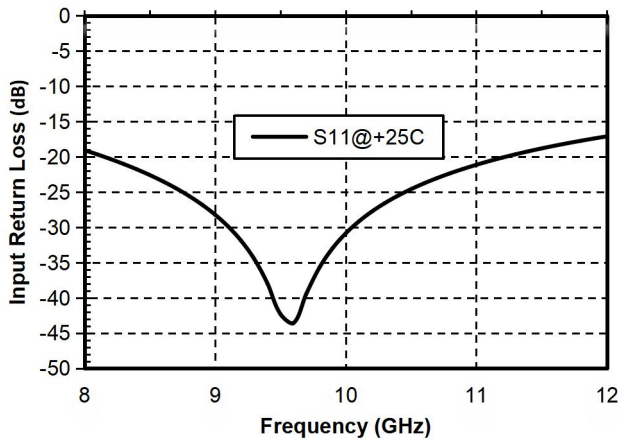
Insertion Loss vs. Operating Frequency



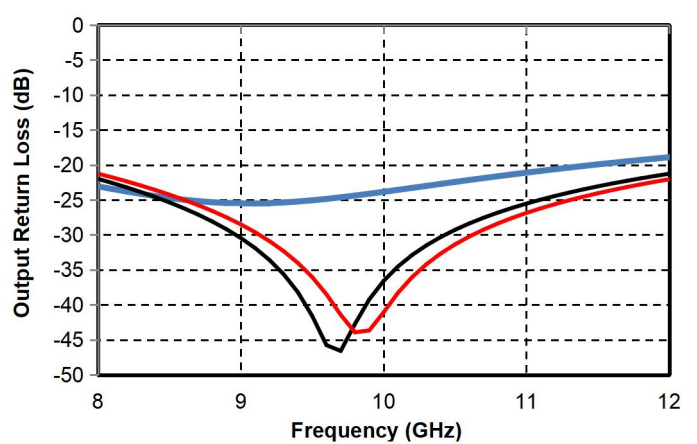
Isolation vs. Operating Frequency



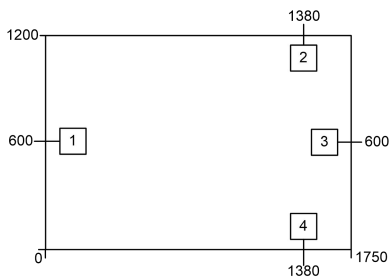
Input Return Loss vs. Operating Frequency



Output Return Loss vs. Operating Frequency






Appearance structure ²

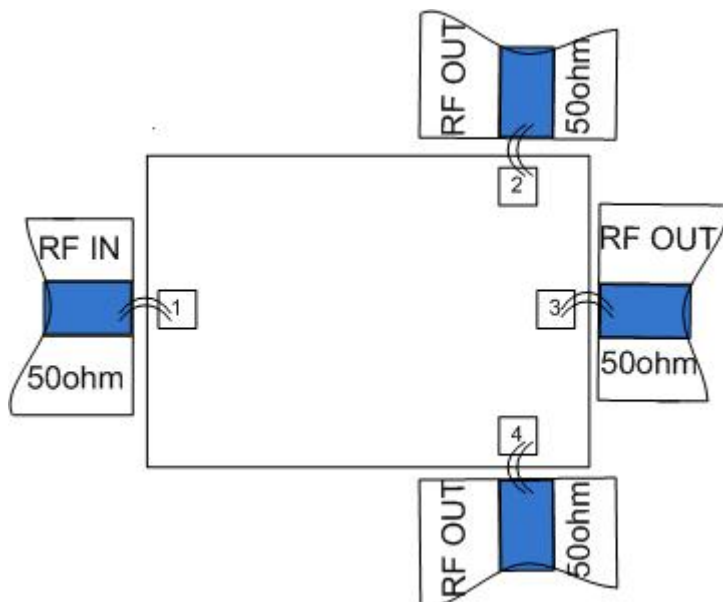


【 2 】 All units in the figure are micrometers

GaAs MMI C Monolithic Integrated 3-way 0-degree Power Divider, 8-12GHz

Bonding point definition			
Bonding point number	Function Symbol	Functional Description	Equivalent Circuit
1	RF IN	RF signal input terminal	
2, 3, 4	RF OUT	RF signal output terminal	
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC	

Recommended assembly drawing



Precautions for use

- The chip needs to be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly comply with ESD protection requirements to avoid electrostatic damage to bare chips.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20 .

The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C. When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C. Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.

- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position , the conductive glue should be vaguely visible around it . For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use $\Phi 0.025\text{mm}$ (1mil) gold wire for both ball and wedge bonding. Thermo-ultrasonic bonding temperature is 150 °C. The pressure of the wedge for ball bonding is 40~50gf , and the pressure of the wedge bonding is 18~22gf . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate) .