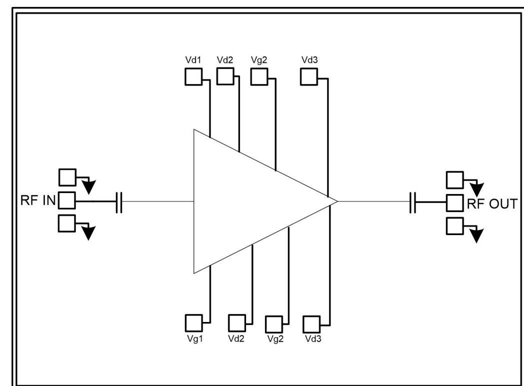
GPA-3337-28

GaAs MMIC Power Amplifier Chip，33-37GHz

Performance characteristics

Frequency range: 33-37GHz
Small signal gain: 15dB
P-1dB: 27dBm
Psat: 28dBm
Power supply:+5.5V/650mA
50Ohm input/output
100% on-chip testing
Chip size: 2.6 x 2.2 x 0.1 mm

Functional Block Diagram



Product Introduction

GPA-3337-28 is a broadband medium power amplifier chip based on GaAs technology, with a frequency range of 33GHz~37GHz, a small signal gain of 15dB, and a saturated output power of 28dBm. The chip through-hole metallization process ensures good grounding, and the back is metallized, suitable for eutectic sintering or conductive adhesive bonding processes.

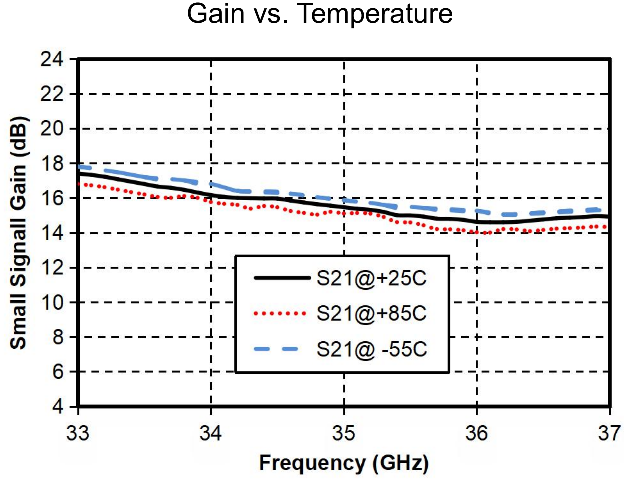
Usage restriction parameter 1	
Maximum leakage voltage	+7V
Maximum gate bias voltage	-3V
Maximum input power	+18dBm
working temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of the above maximum limits may result in permanent damage.

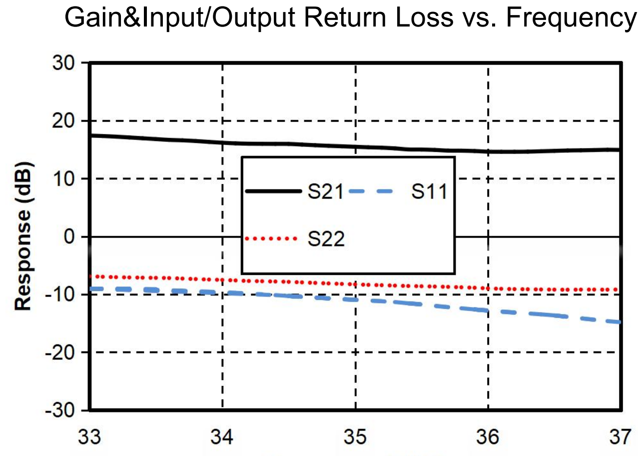
Electrical performance parameters(T_A = +25°C，Vd=+5.5V)				
index	Minimum	Typical Value	Maximum	unit
Frequency range		33-37		GHz
Small signal gain	14.5	15	16	dB
Gain flatness		±0.75		dB
P-1dB	27.0	27.5	28.5	dBm
Psat	27.5	28	28.8	dBm
input return loss		11		dB
Output Return Loss		8		dB
Static current		650		mA
By tuning the Vg terminal voltage to -2V~0V, it reaches 650mA.				

Main index test curve

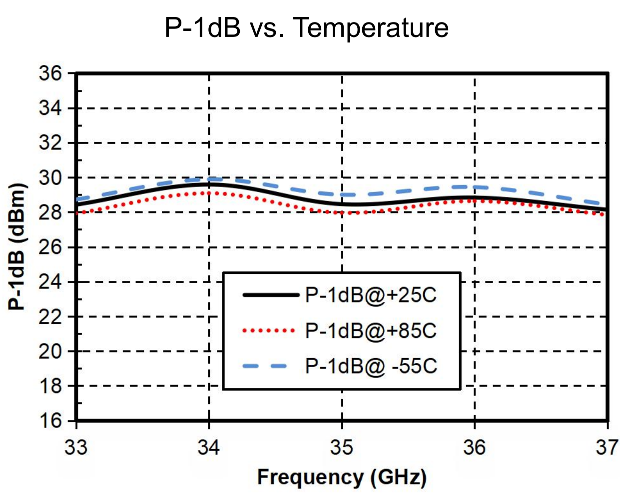
Gain vs. Temperature



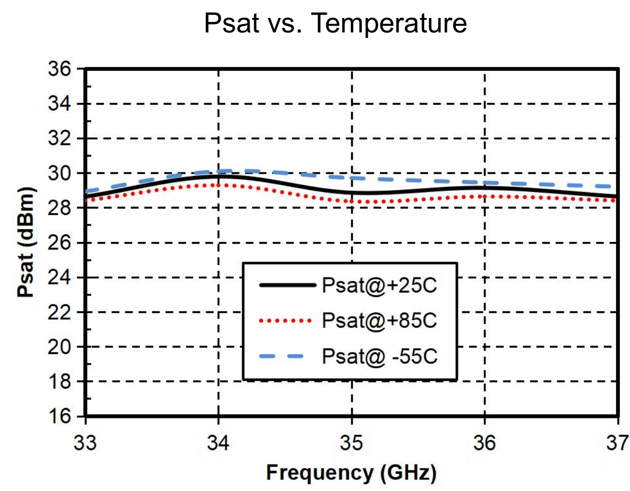
Gain&Input/Output Return Loss vs. Frequency



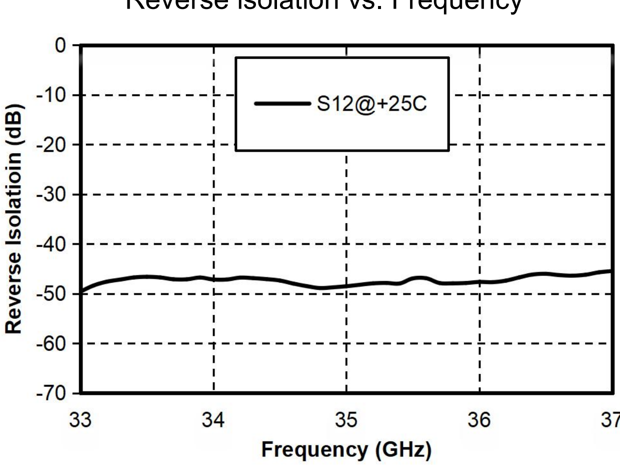
P-1dB vs. Temperature



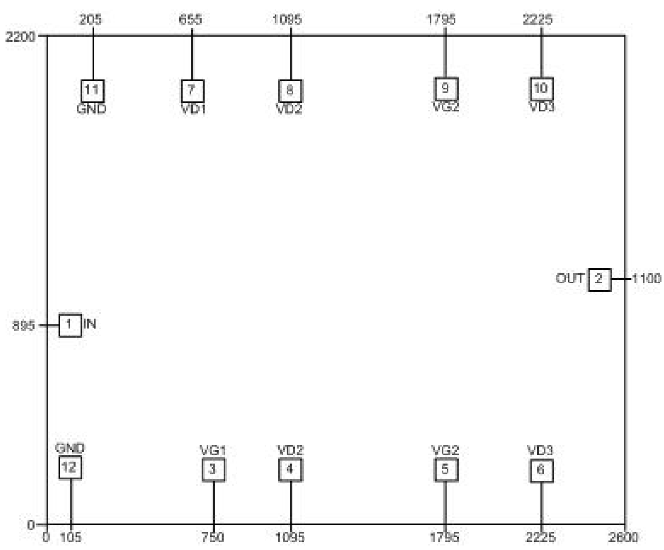
Psat vs. Temperature



Reverse isolation vs. Frequency



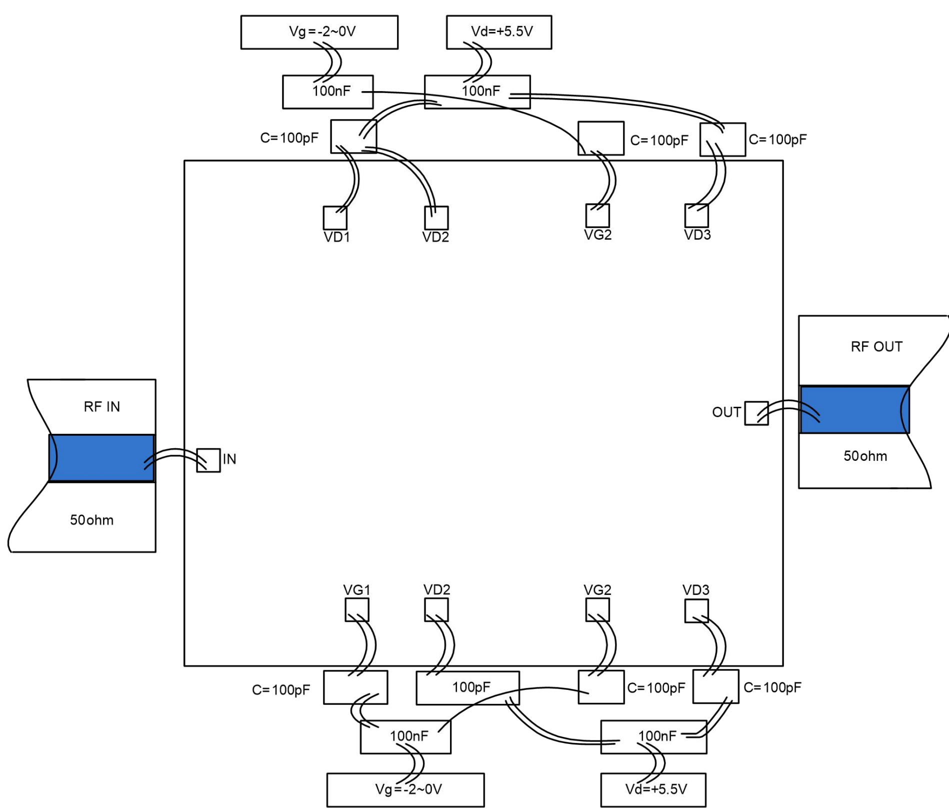
External Structure 2



【2】 The units in the figure are all micrometers.

Definition of bonding pressure point			
Bonding point number	Function Symbol	Functional Description	Equivalent circuit
1	RFIN	RF signal input terminal, no need for DC capacitors	RF IN
2	RFOUT	RF signal output terminal, no need for DC isolation capacitor	RF OUT
7	Vd1	Amplifier drain bias, requires external 100pF, 100nF bypass capacitors	Vdd
4、8	Vd2	Amplifier drain bias, requires external 100pF, 100nF bypass capacitors	Vdd
6、10	Vd3	Amplifier drain bias, requires external 100pF, 100nF bypass capacitors	Vdd
3	Vg1	Amplifier gate bias, requires external 100pF, 100nF bypass capacitors	Vg
5、9	Vg2	Amplifier gate bias, requires external 100pF, 100nF bypass capacitors	Vg
11、12	GND	Grounding pressure point	GND
芯片底部	GND	The bottom of the chip needs to be well grounded with RF and DC	GND

Suggested assembly diagram



Notice

- The chip needs to be stored in a container with anti-static function and stored in a nitrogen environment.
- Attempting to clean the surface of bare chips using wet chemical methods is prohibited.
- Please strictly comply with ESD protection requirements to avoid static damage to bare chips.
- Routine operation: Please use precision pointed tweezers to remove the bare chip. During the operation, avoid tools or fingers touching the surface of the chip.
- Suggestion for mounting operation: Bare chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold tin ratio of 80/20. The working surface temperature reached 255 ℃, and the tool (vacuum chuck) temperature reached 265 ℃. When a high-temperature mixed gas (nitrogen to hydrogen ratio of 90/10) is blown onto the chip, the temperature at the top of the tool should be raised to 290 ℃. Do not let the chip stay above 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive adhesive applied should be as small as possible.

After placing the chip in the installation position, the conductive adhesive can be vaguely visible around it. Please follow the information provided by the conductive adhesive manufacturer for curing conditions.

- Suggestion for bonding operation: Both spherical or wedge-shaped bonding should be used Φ 0.025mm (1mil) gold wire. Thermal ultrasonic bonding temperature is 150 ℃. The pressure of the spherical bonding cutter is 40-50GF, and the pressure of the wedge bonding cutter is 18-22GF. Use as little ultrasonic energy as possible. The bonding process starts at the pressing point on the chip and ends at the packaging (or substrate).