

GaAs MMIC Power Amplifier Chip, 32-42GHz

Performance characteristics

Frequency range: 32-42GHz

Small Signal Gain: 22dB

P-1dB: 24.5dBm

Psat: 25dBm

Power supply: +5V@210mA

50Ohm input/output

100% on-chip testing

Chip size: 2.12 x 1.1 x 0.1mm

Product Introduction

GPA-3242A is a broadband amplifier chip based on GaAs technology, covering a frequency range of 32-44GHz, with a small signal gain of 22dB and a Psat output power of 25.5dBm. The chip supports +6V operation. The chip via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

Use restriction parameter ¹

Maximum drain voltage	+7 V
Maximum input power	+20 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd = +5 V , Ids= 210 mA)

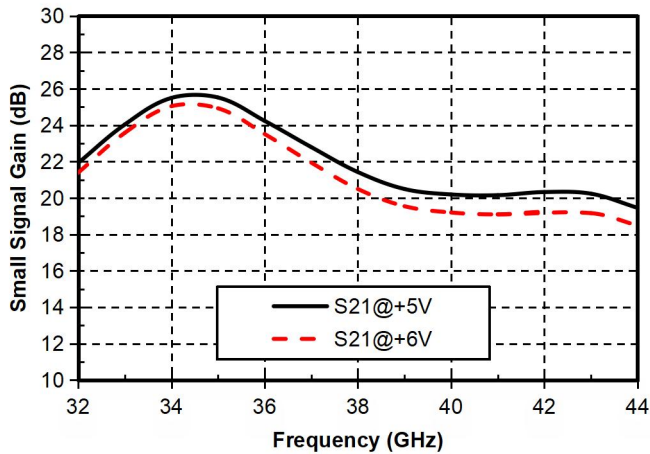
index	Minimum	Typical Value	Maximum	unit
Frequency Range	32-42			GHz
Small Signal Gain	-	22	-	dB
Gain Flatness	± 2.5			dB
P-1dB	-	24.5	-	dBm
Psat	-	25	-	dBm
Input return loss	-	13	-	dB
Output return loss	-	7	-	dB

*By tuning the Vg terminal voltage from -2V to 0V, the recommended Vg terminal voltage is -0.75V .

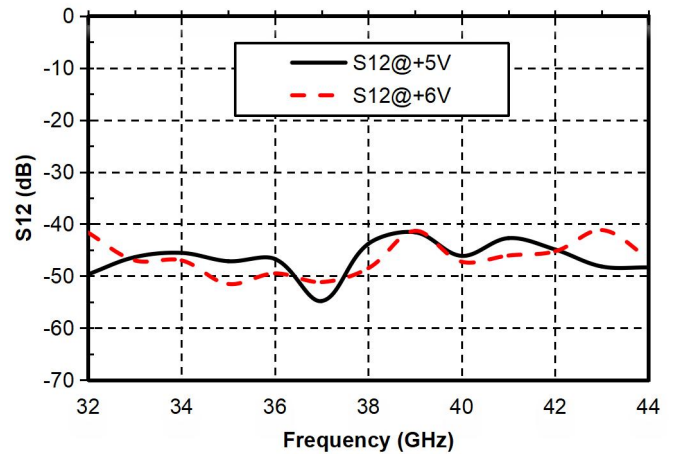
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Main index test curve

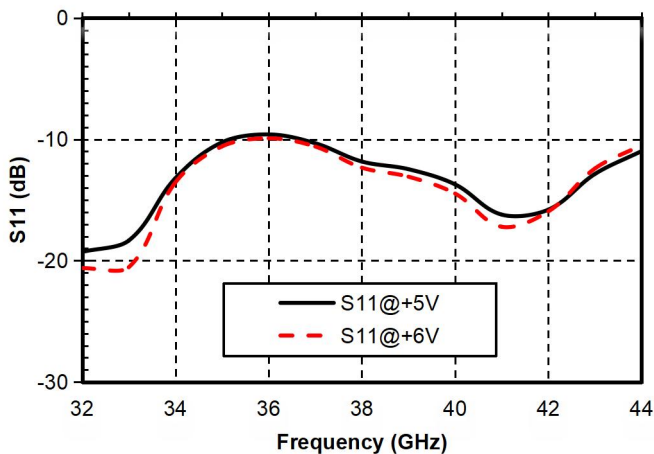
Gain vs. Frequency



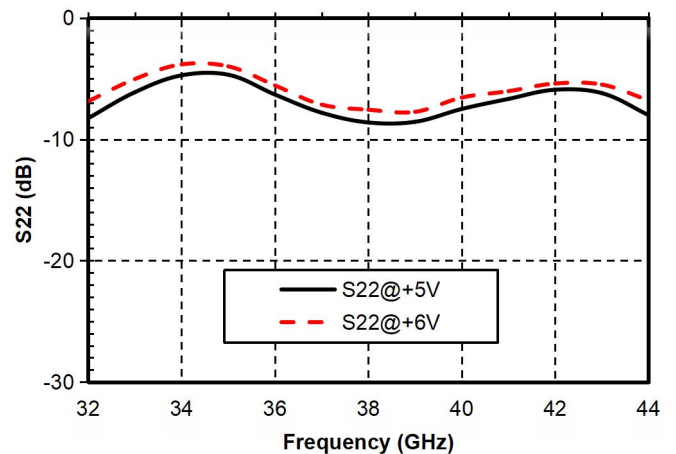
Reverse Isolation vs. Frequency



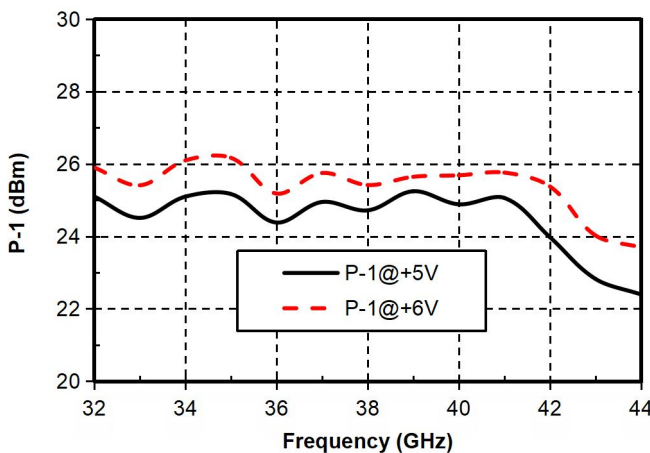
Input Return Loss vs. Frequency



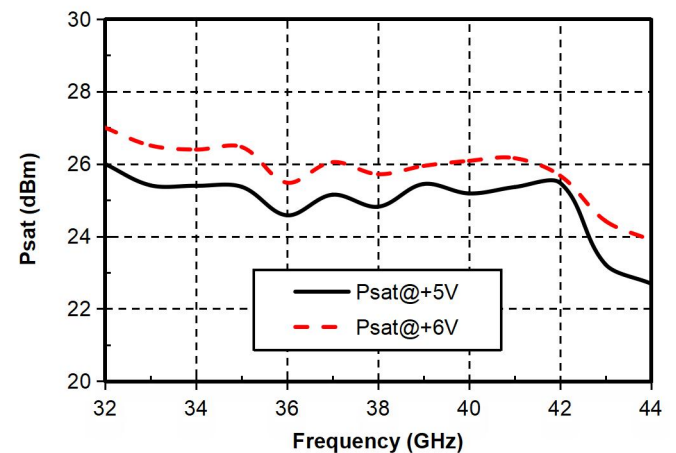
Output Return Loss vs. Frequency



P -1 vs. Frequency

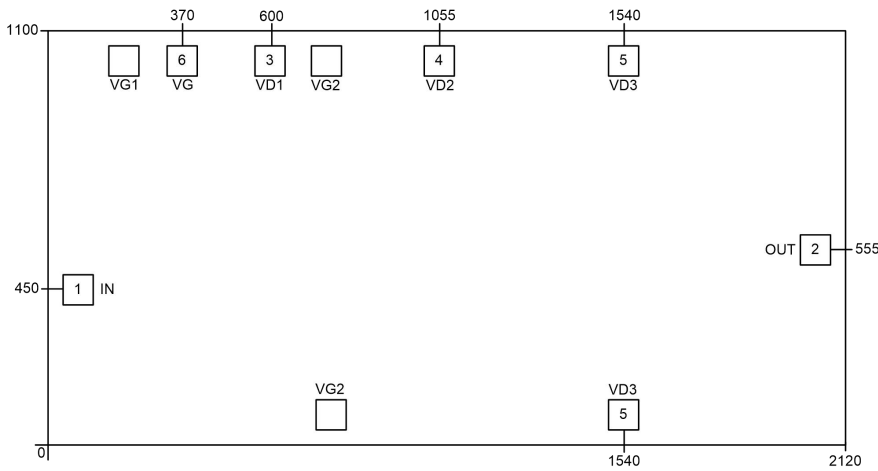


P sat vs. frequency



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Appearance structure ²

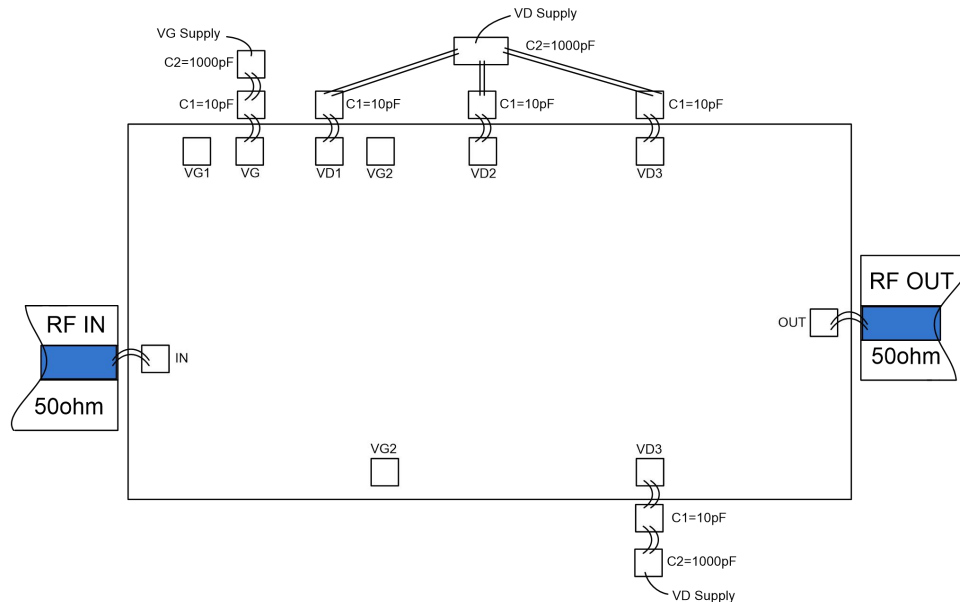


【 2 】 The units in the figure are all micrometers (dimensional tolerance: $\pm 100\mu\text{m}$.)

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required
3~5	VD1 , VD2, VD3	Amplifier drain bias, external 10 pF, 1000pF bypass capacitor required
6	VG1	Amplifier gate bias, external 10 pF, 1000pF bypass capacitor required
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds

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Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C . Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use $\Phi 0.025\text{mm}$ (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 °C . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).