

GaAs MMIC Power Amplifier Chip, 20-40GHz

Performance characteristics

Frequency range: 20-40GHz

Small Signal Gain: 22.5 dB

Gain flatness: $\leq \pm 1.75$ dB

Noise figure: 7.0dB typ.

P-1dB: 21dBm

Psat: 23dBm

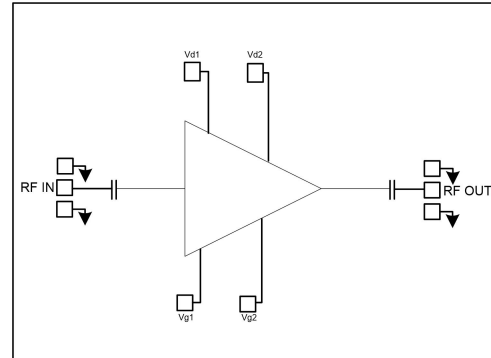
Power supply: +5 V/ 180 mA

50Ohm input/output

100% on-chip testing

Chip size: 1.85 x 1.05 x 0.1mm

Functional Block Diagram



Product Introduction

GPA-2040B is a broadband amplifier chip based on GaAs technology, covering a frequency range of 20 ~ 40 GHz, a small signal gain of 21dB, and a saturated output power of 23dBm. The chip is powered by a +5V power supply. The chip through-hole metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding process.

Use restriction parameter ¹

Maximum drain voltage	+7 V
Maximum gate bias	-3V
Maximum input power	+20dBm
Operating temperature	-55 ~ + 85 °C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , Vd = +5V)

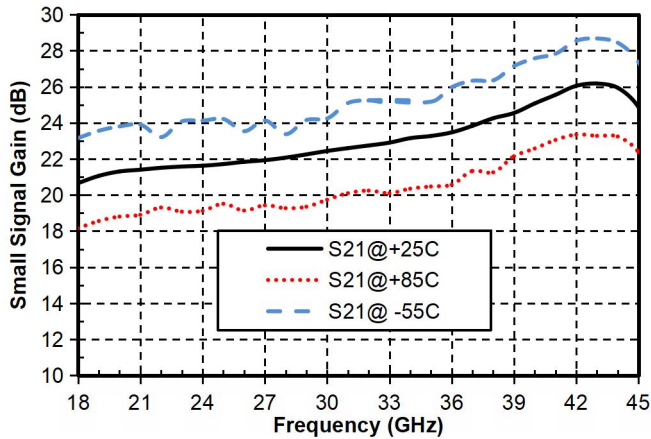
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	20-40			GHz
Small Signal Gain	-	22.5	-	dB
Gain Flatness	± 1.75			dB
P -1 dB	-	21	-	dBm
Psat	-	23	-	dBm
Input return loss	-	17	-	dB
Output return loss	-	10	-	dB
Quiescent Current	180			mA

* By tuning the Vg terminal voltage from -2V to 0V , 180 mA is achieved , and the Vg terminal voltage is expected to be -0.7 V.

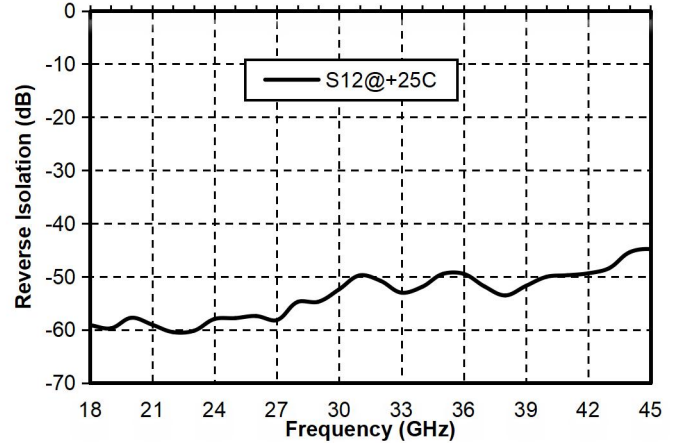
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Main index test curve (the following data is based on probe test)

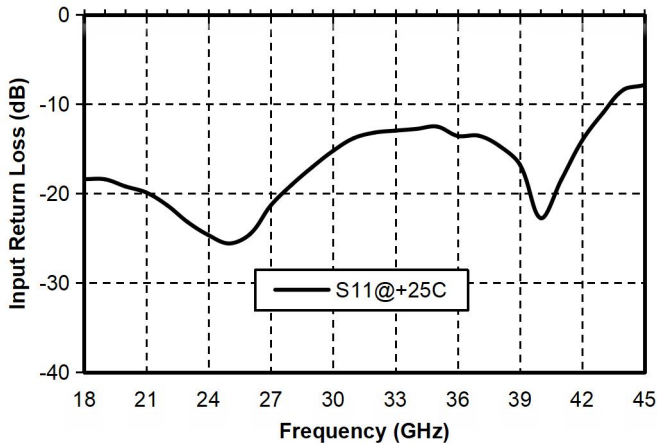
Gain vs. Frequency



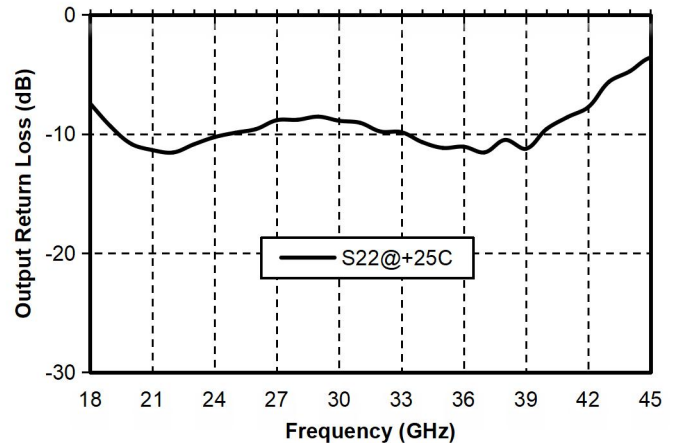
Reverse Isolation vs. Frequency



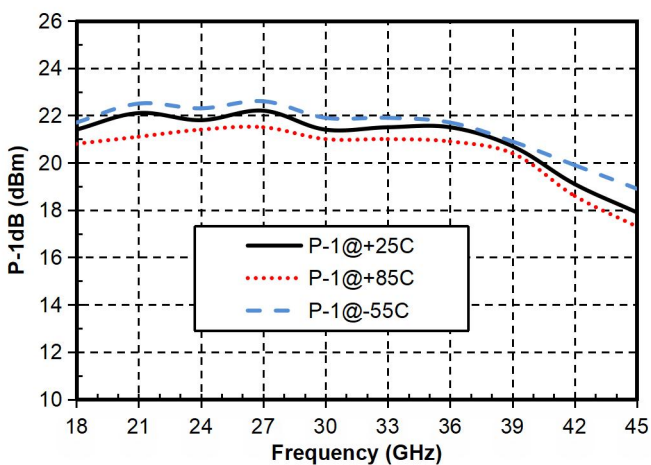
Input Return Loss vs. Frequency



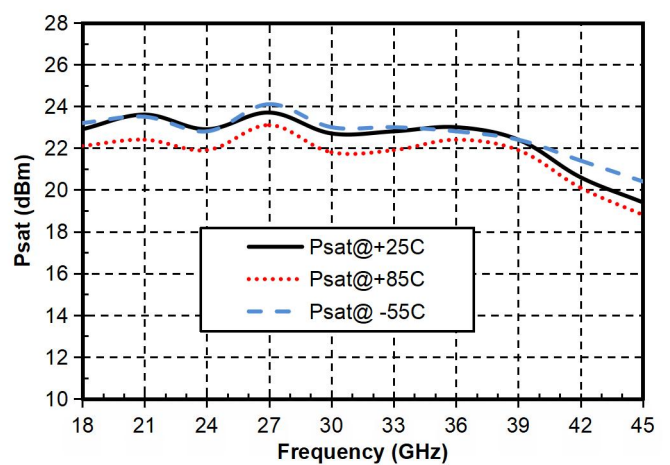
Output Return Loss vs. Frequency



P-1dB vs. Frequency

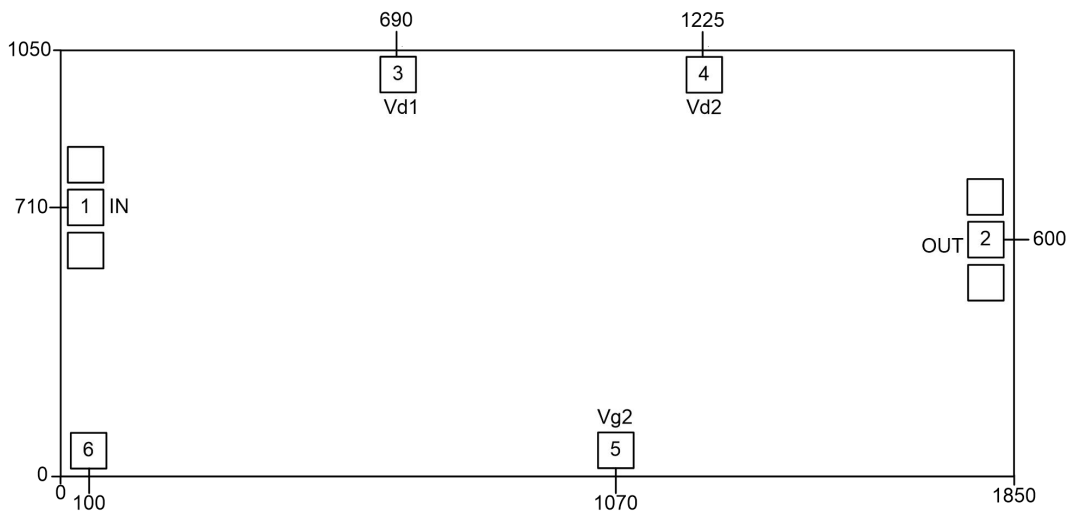


Psat vs. Frequency



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Appearance structure ²



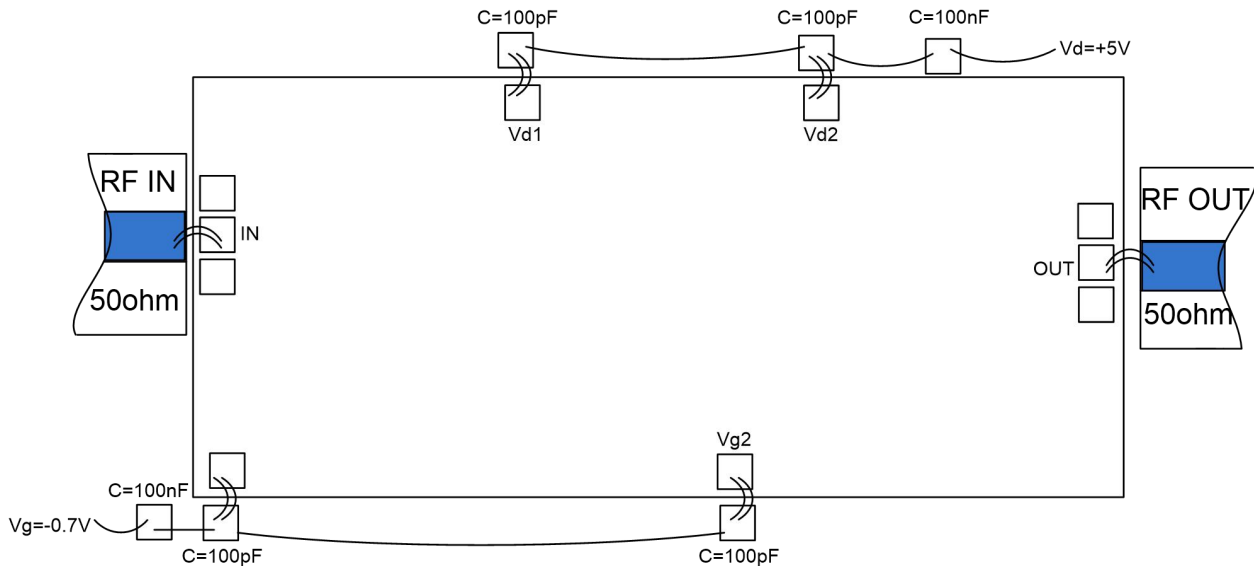
【 2 】 All units in the figure are micrometers

Bonding point definition

Bonding point number	Function Symbol	Functional Description
1	RF IN	RF signal input terminal, no DC blocking capacitor required
2	RF OUT	RF signal output terminal, no DC blocking capacitor required
3,4	Vd 1, Vd 2	Amplifier drain bias, requires external 100 pF, 1000pF, 100nF bypass capacitor
5, 6	Vg1, Vg2	Amplifier gate bias, external 100 pF, 1000 pF, 100 nF bypass capacitor required
Chip bottom	GND	needs to be in good contact with the RF and DC grounds

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Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C . Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position, the conductive glue can be vaguely seen around it . For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use $\Phi 0.025\text{mm}$ (1mil) gold wire for both ball and wedge bonding . Thermosonic bonding temperature is 150 °C . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).