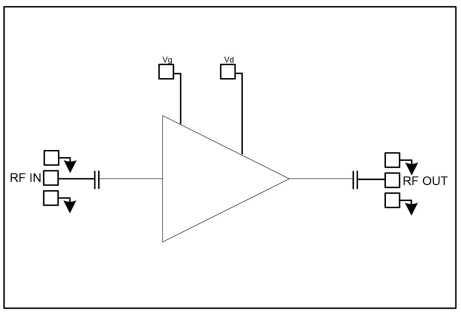
GPA-1850C

GaAs MMIC Power Amplifier Chip, 18-50GHz

Performance characteristics

Frequency range: 15 - 50 GHz
Small Signal Gain: 18.5 dB
P-1dB: 16.5 dBm
Psat: 17.5 dBm
Power supply: +5V@115mA
50Ohm input/output
100% on-chip testing
Chip size : 1.92 x 1.25 x 0.1mm

Functional Block Diagram



Product Introduction

GPA-1850C is a broadband amplifier chip based on GaAs technology, covering a frequency range of 18~50GHz, with a small signal gain of 18.5dB and a P-1 output power of 16.5dBm. The chip via metallization process ensures good grounding, and the back side is metallized for eutectic sintering process.

Use restriction parameter [1]	
Maximum drain voltage	+7 V
Maximum input power	+20 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd= +5 V , Ids= 115 mA)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range		18-50		GHz
Small Signal Gain	-	18.5	-	dB
Gain Flatness		± 1.75		dB
P-1dB	-	16.5	-	dBm
Psat	-	17.5	-	dBm
Input return loss	-	14.5	-	dB
Output return loss	-	19	-	dB

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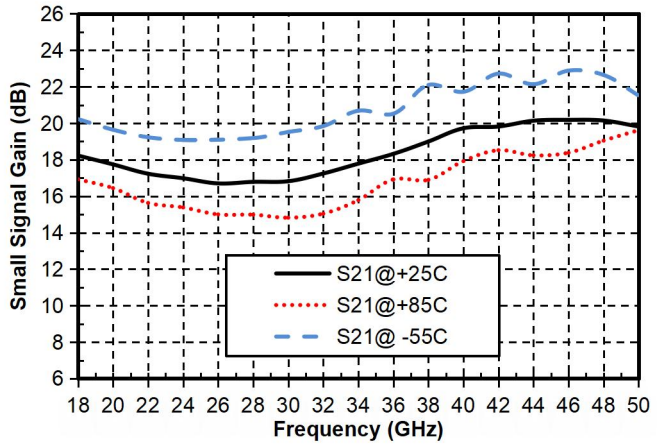
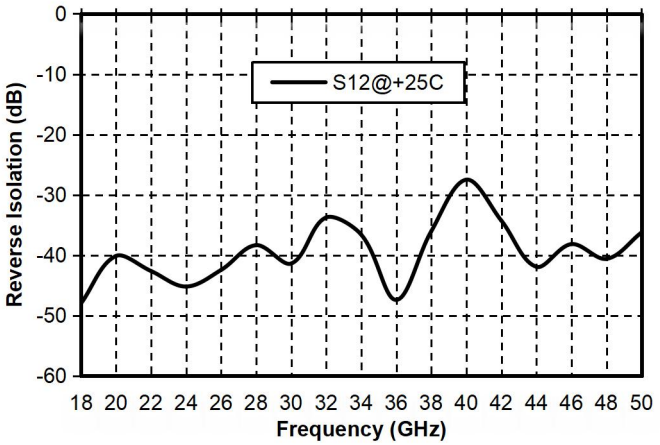
Main index test curve

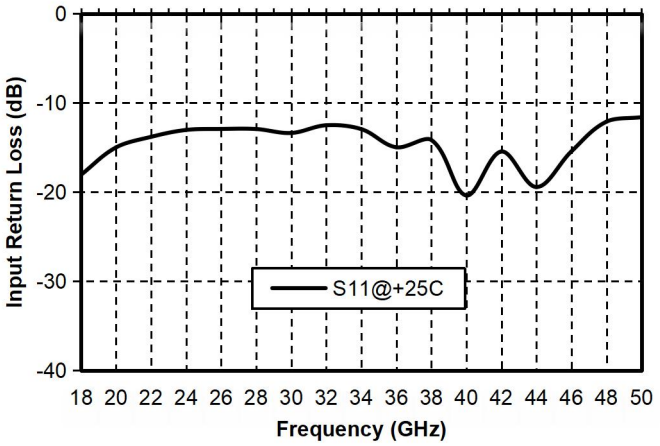
Gain vs. Frequency



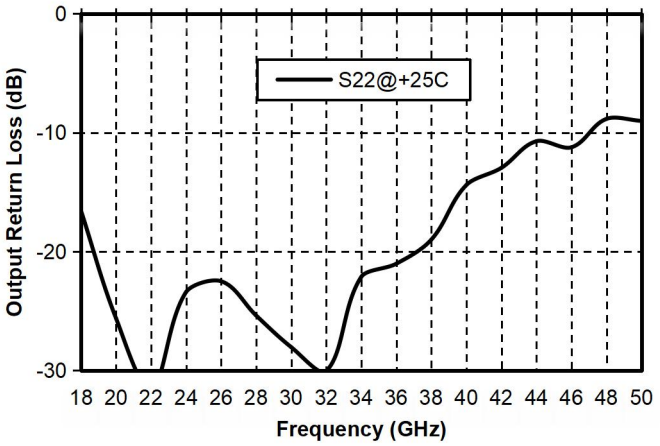
Reverse Isolation vs. Frequency



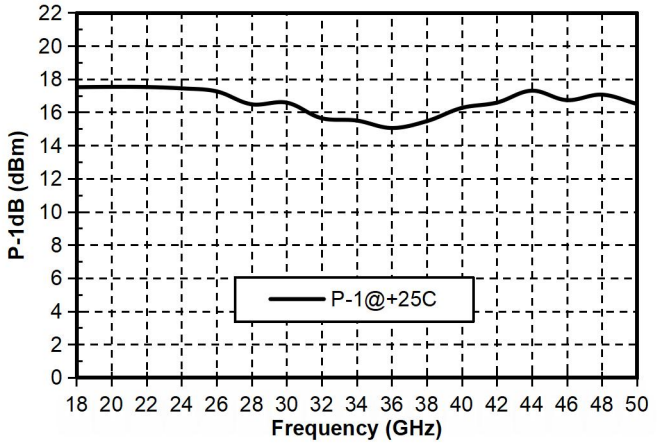
Input Return Loss vs. Frequency



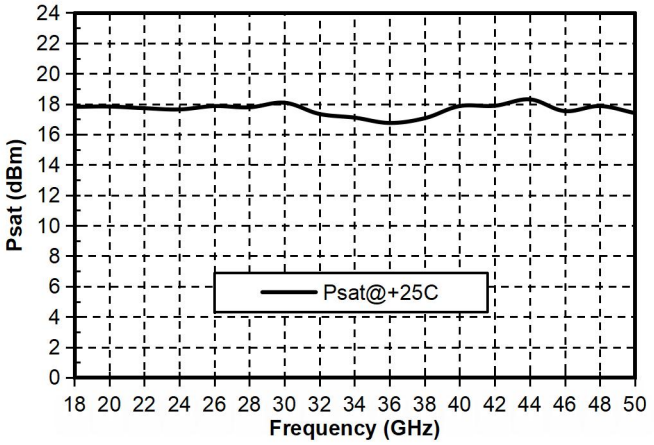
Output Return Loss vs. Frequency



P-1dB vs. Frequency



Psat vs. Frequency



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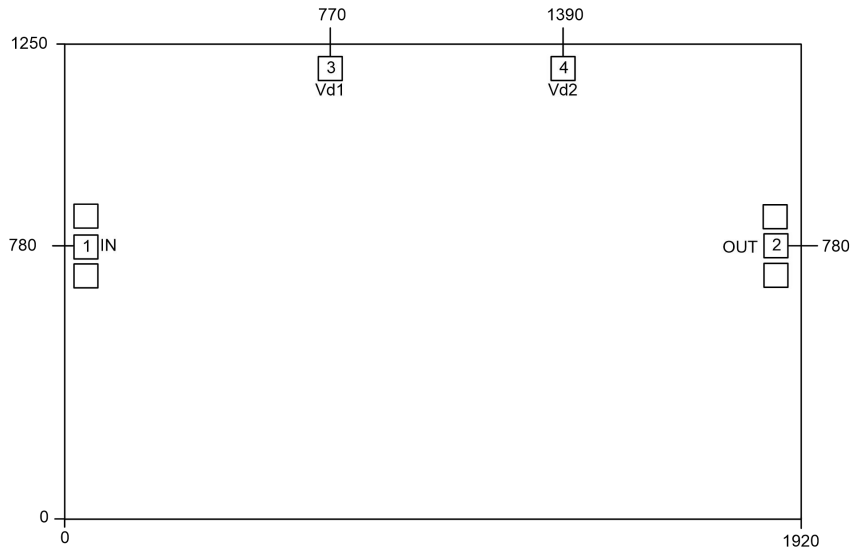
Appearance structure [2]



【2】The units in the figure are all micrometers (dimensional tolerance: ±100um.)

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required
3.4	VD1 , VD2	Amplifier drain bias, external 100 nF, 100pF bypass capacitor required
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds

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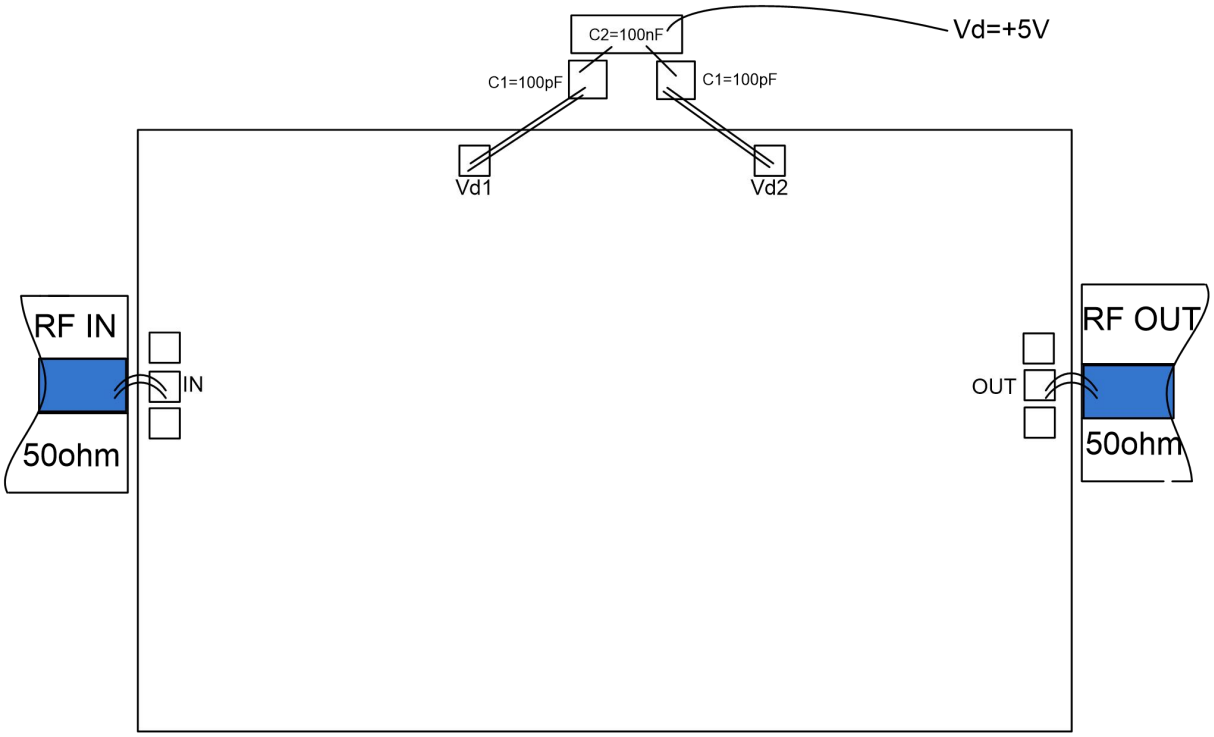
Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).