GPA-1750B

GaAs MMIC Power Amplifier Chip, 17-50GHz

Performance characteristics

Frequency range: 17-50GHz
Small Signal Gain: 18.5 dB
P-1dB: 23dBm
Psat: 24dBm
Power supply: +5 V/ 380 mA
50Ohm input/output
100% on-chip testing
Chip size: 2.32 x 1.59 x 0.1mm

Product Introduction

GPA-1750B is a broadband amplifier chip based on GaAs technology, covering a frequency range of 17-50GHz, a small signal gain of 18.5dB, and a saturated output power of 24dBm. The chip is powered by a +5V power supply. The chip through-hole metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding.

Use restriction parameter [1]	
Maximum drain voltage	+7 V
Maximum gate bias	-3V
Maximum input power	+20dBm
Operating temperature	-55 ~ + 85 °C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , Vd = +5V)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range		18-50		GHz
Small Signal Gain	-	18.5	-	dB
Gain Flatness		± 5.0		dB
P -1 dB		23		dBm
Psat		24		dBm
Input return loss	-	15	-	dB
Output return loss	-	20	-	dB
Quiescent Current		380		mA
* By tuning the Vg terminal voltage from -2V to 0V , 380 mA is achieved , and the Vg terminal voltage is expected to be -0.7 V.				

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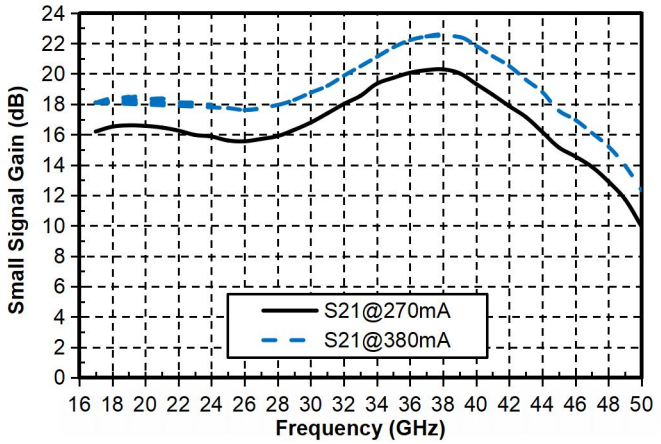
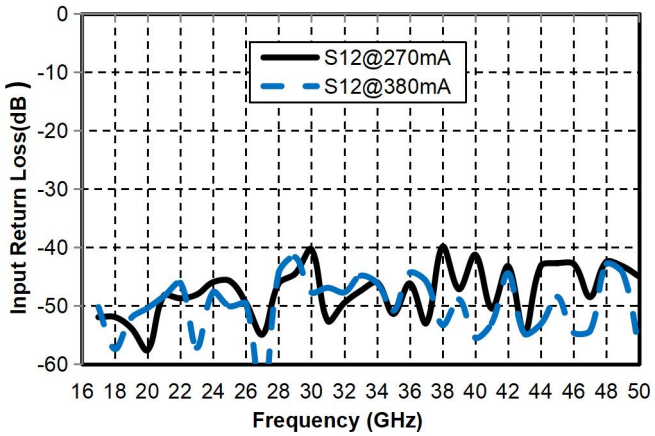
Main index test curve (the following data is based on probe test)

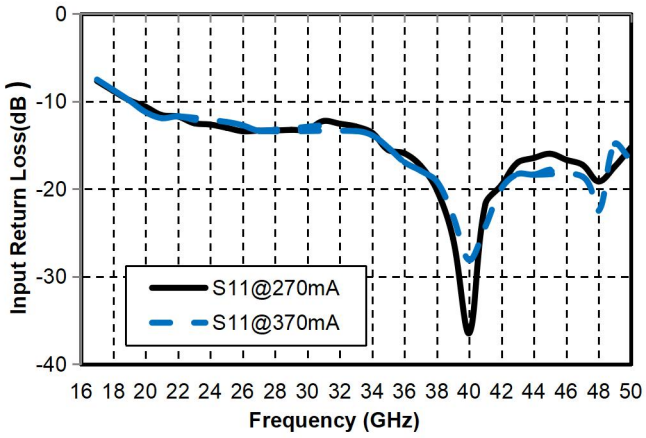
Gain vs. Frequency



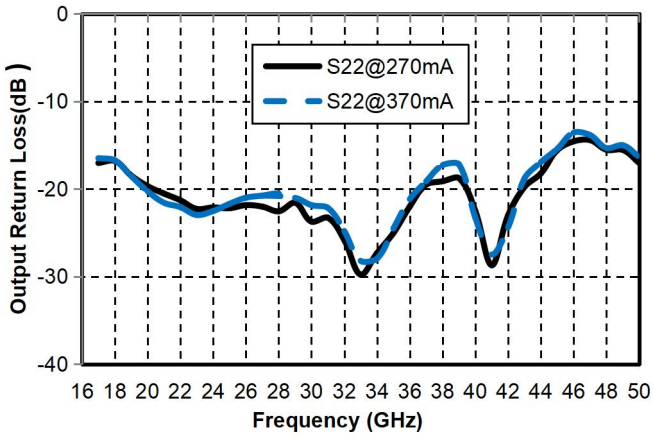
Reverse Isolation vs. Frequency



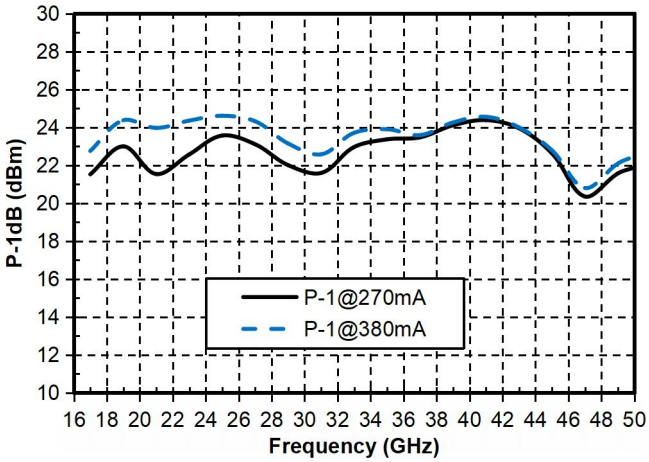
Input Return Loss vs. Frequency



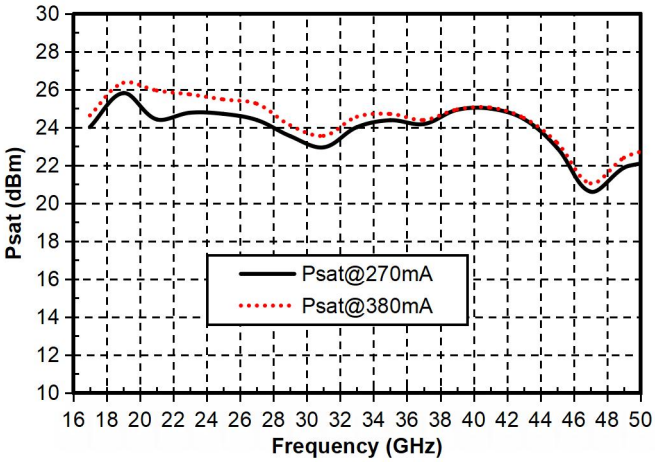
Output Return Loss vs. Frequency



P-1dB vs. Frequency



Psat vs. Frequency



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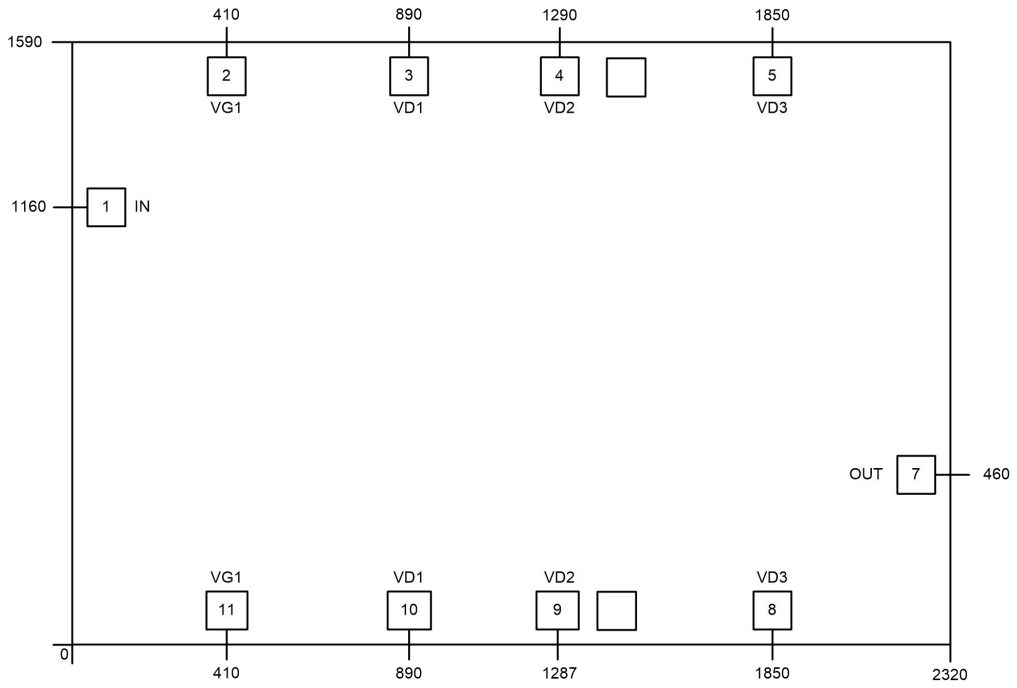
Appearance structure [2]



【 2 】All units in the figure are micrometers

Bonding point definition

Bonding point number	Function Symbol	Functional Description
1	RF IN	RF signal input terminal, no DC blocking capacitor required
2	RF OUT	RF signal output terminal, no DC blocking capacitor required
2.11	VG1	Amplifier drain bias, external 10pF , 1000pF bypass capacitor required
3, 4, 5, 8, 9, 10	VD1~VD3	Amplifier gate bias, external 10pF , 1000pF bypass capacitor required
Chip bottom	GND	needs to be in good contact with the RF and DC grounds

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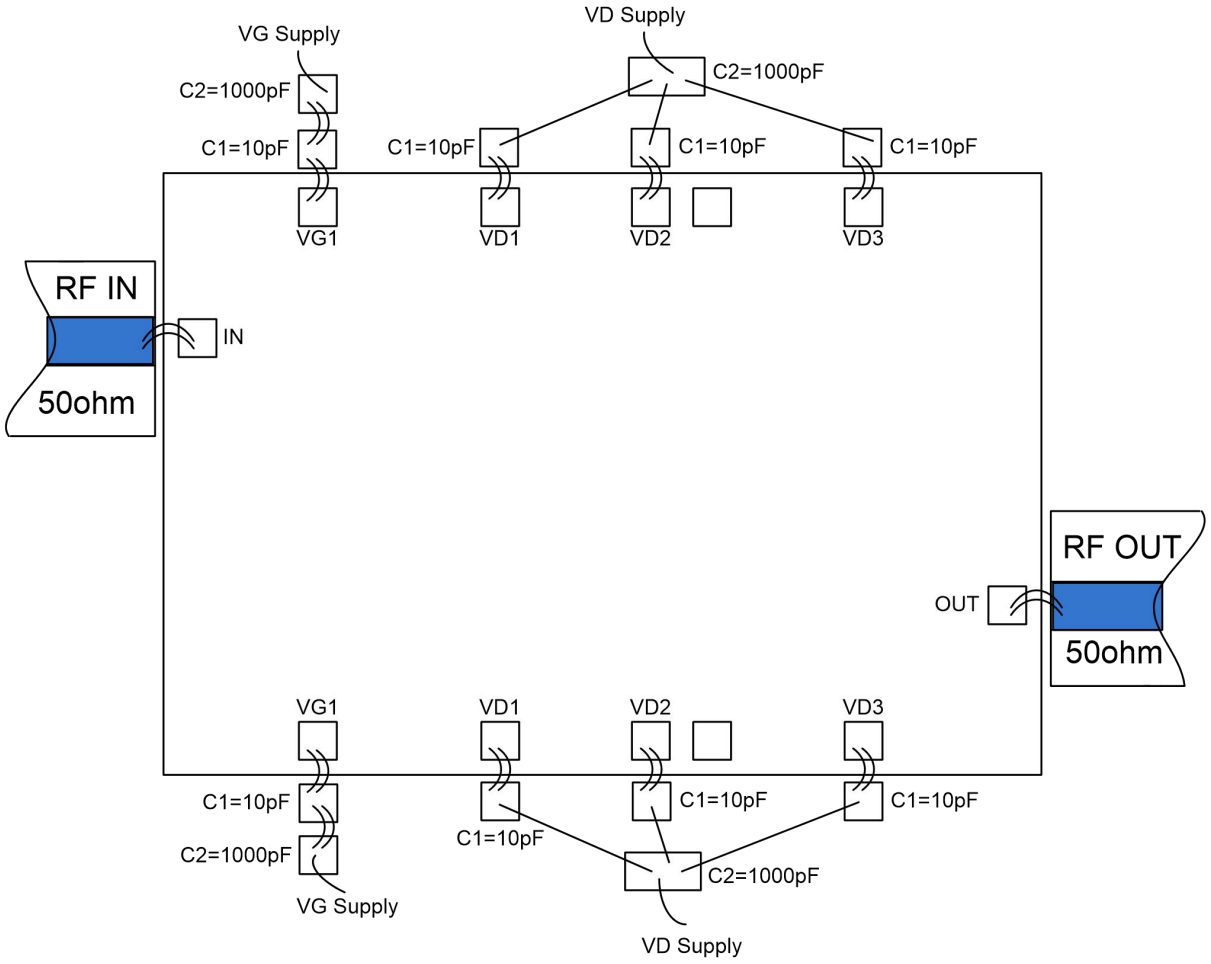
Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more

than 20 seconds. The friction time should not exceed 3 seconds.

- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position, the conductive glue can be vaguely seen around it . For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding . Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).