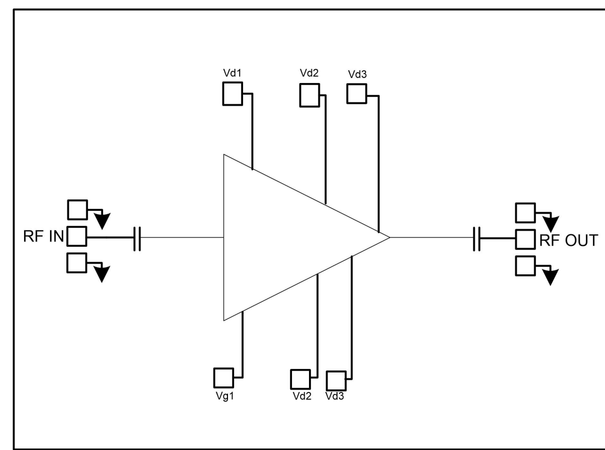
GPA-1517-35A

GaAs MMIC Power Amplifier Chip, 15-17GHz

Performance characteristics

Frequency range: 15-17GHz
Small Signal Gain: 26 dB
Power gain: 23dB
P-1dB: 34.5 dBm
Psat: 35 dBm
PAE: 36%~39%
Power supply: +7 V / 600 mA
50Ohm input/output
100% on-chip testing
Chip size : 2.75 x 1.6 x 0.1mm

Functional Block Diagram



Product Introduction:

GPA-1517-35A is a high-gain, high-efficiency, high- power amplifier chip based on GaAs technology , covering a frequency range of 15~17GHz, with a small signal gain of 26dB, a power gain of 23dB, a saturated output power of 35 dBm, and an additional efficiency of 36%~39% . The chip via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

Use restriction parameter [1]	
Maximum drain voltage	+8 V
Maximum gate bias	- 3 V
Maximum input power	+17 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd=+ 7 V, Ids= 600 mA)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range	15 - 17			GHz
Small Signal Gain	25.5	26	26.5	dB
Gain Flatness	± 0.5			dB
P-1dB	34	34.5	34.7	dBm
Psat	34.5	35	35	dBm
Input return loss	-	14	-	dB
Output return loss	-	16	-	dB
* By adjusting the Vg terminal voltage from -2V to 0V , the Ids reaches 600 mA . The recommended gate voltage is -0.9V.				

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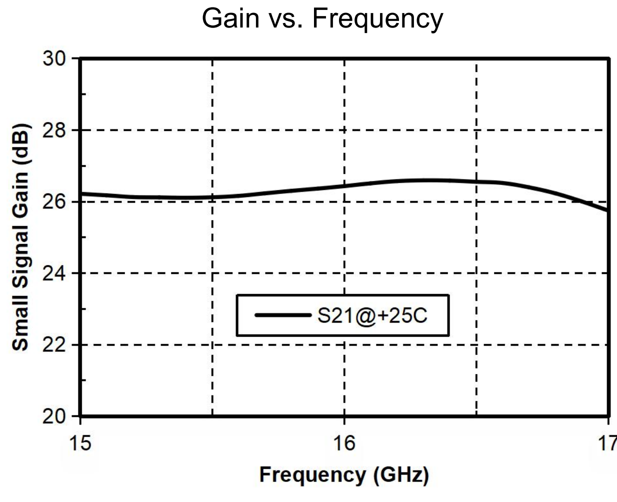
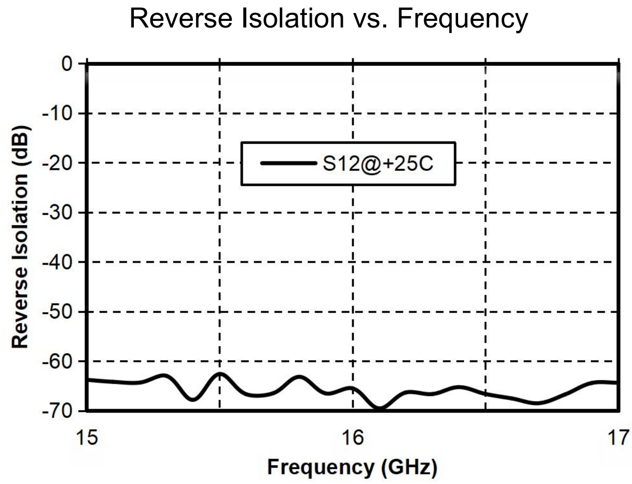
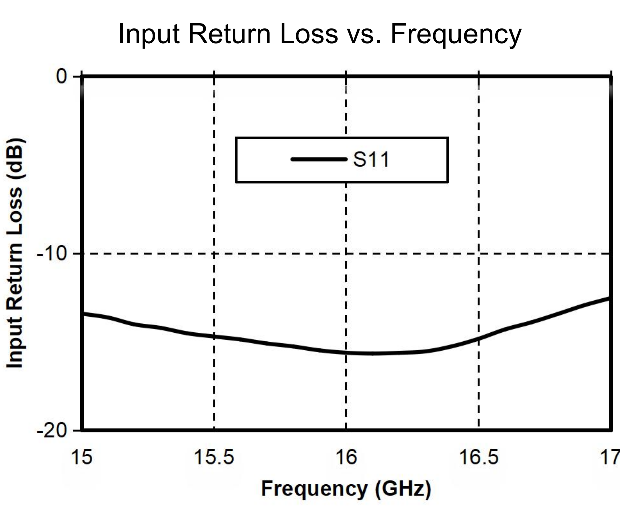
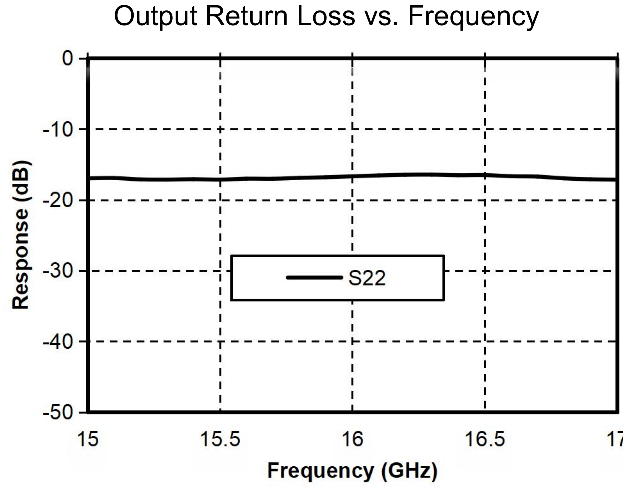
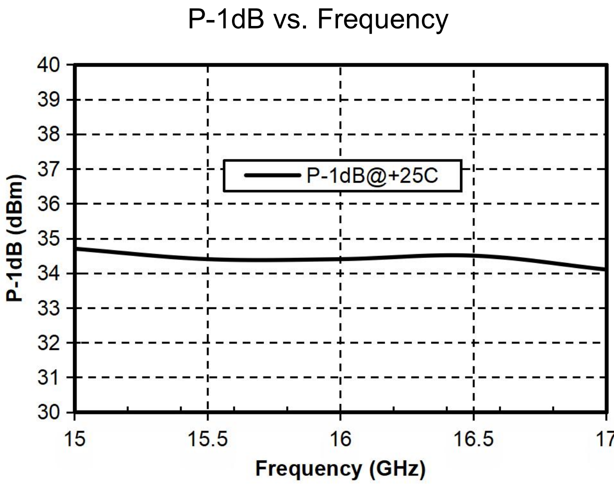
Main index test curve

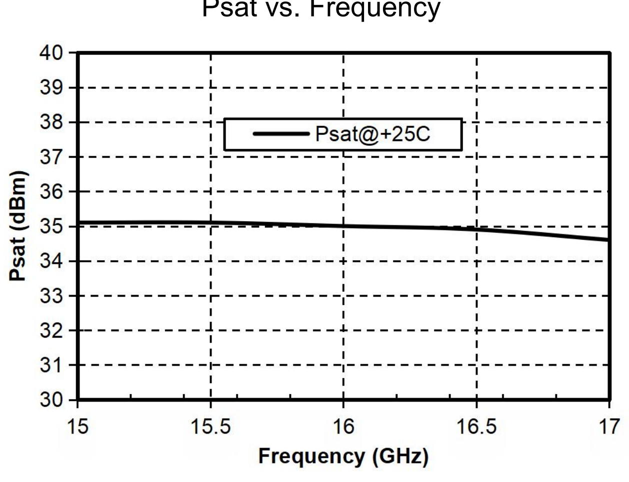












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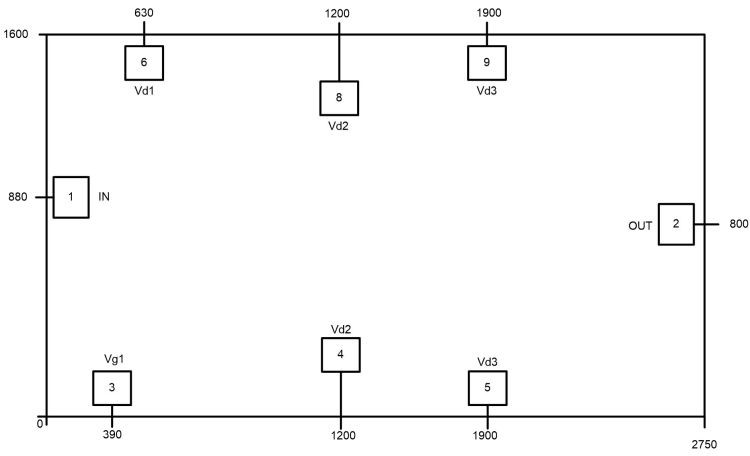
Appearance structure [2]



【 2 】All units in the figure are micrometers

Bonding point definition			
Bonding point number	Function Symbol	Functional Description	Equivalent Circuit
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required	RF IN
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required	RF OUT
4, 5, 6, 8, 9	Vd 1~4	Amplifier drain bias, external 100pF, 0.1uf F, 4.7uF bypass capacitors are required	Vdd
3	Vg1	Amplifier gate bias, external 100pF, 0.1uf F, 4.7uF bypass capacitors are required	Vg
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds	GND

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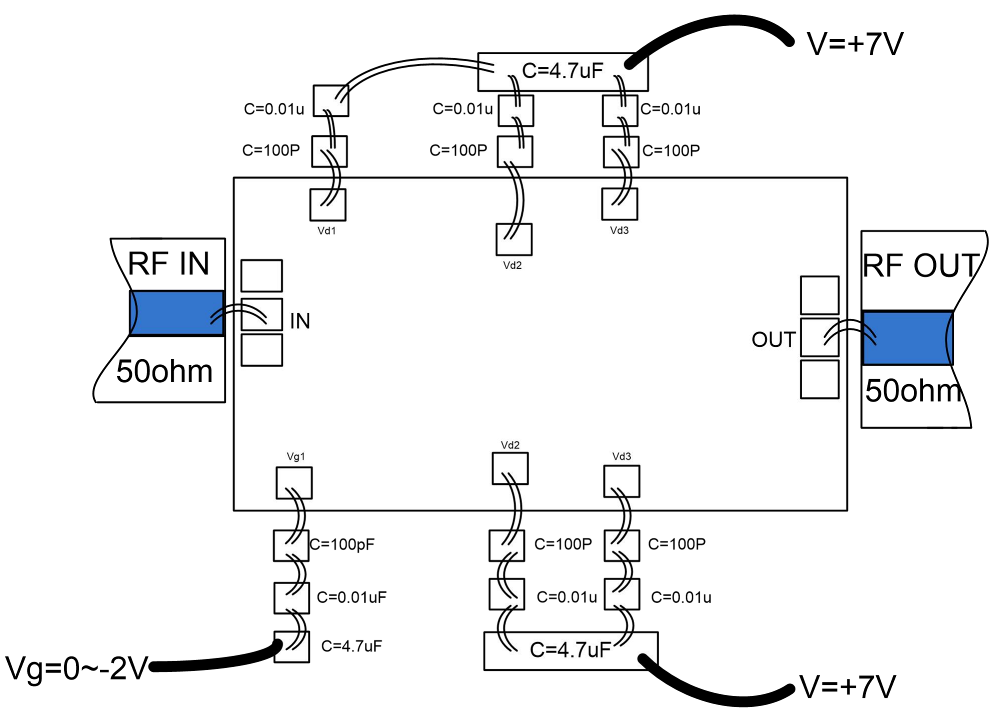
Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).

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