# GPA-1517-35

## GaAs MMIC Power Amplifier Chip, 15-17GHz

### Performance characteristics

Frequency range: 15-17GHz
Small Signal Gain: 37 dB
Power gain: 34dB
P-1dB: 34 dBm
Psat: 35 dBm
PAE: 38%~40%
Power supply: 7 V/ 660 mA
50Ohm input/output
100% on-chip testing
Chip size : 3.3 x 1.6 x 0.1mm

### Product Introduction:

GPA -1517-35 is a high-gain, high-efficiency, high- power amplifier chip based on GaAs technology , covering a frequency range of 15~17GHz, with a small signal gain of 37dB, a power gain of 34dB, a saturated output power of 35dBm, and an additional efficiency of 38%~40% . The chip via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

| Use restriction parameter [1] | |
|---|---|
| Maximum drain voltage | +8 V |
| Maximum gate bias | - 3 V |
| Maximum input power | +10 dBm |
| Operating temperature | -55 ~ +85°C |
| Storage temperature | -65 ~ +150°C |

【1】 Exceeding any of these maximum limits may cause permanent damage.

| Electrical parameters (Ta=+25°C, Vd = 7V , Ids= 660mA ) | | | | |
|---|---|---|---|---|
| index | Minimum | Typical Value | Maximum | unit |
| Frequency Range | 15 - 17 | | | GHz |
| Small Signal Gain | 36.5 | 37 | 37.5 | dB |
| Gain Flatness | ± 0.5 | | | dB |
| P-1dB | - | 34 | 34.5 | dBm |
| Psat | - | 35 | - | dBm |
| Input return loss | - | 15 | - | dB |
| Output return loss | - | 13 | - | dB |
| * By adjusting the Vg terminal voltage from -2V to 0V , the Ids reaches 660 mA . The recommended gate voltage is -0.9V. | | | | |

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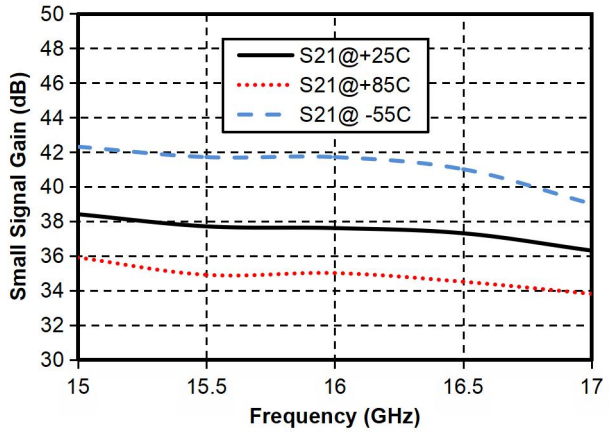
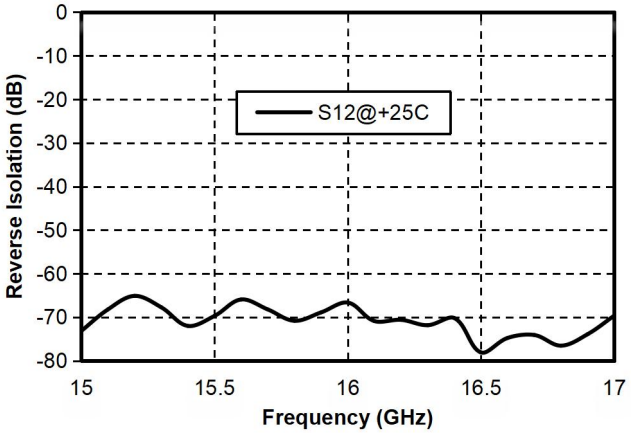
## Main index test curve

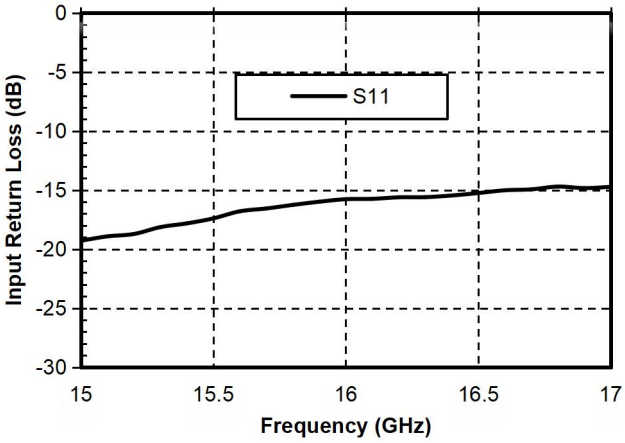
Gain vs. Frequency



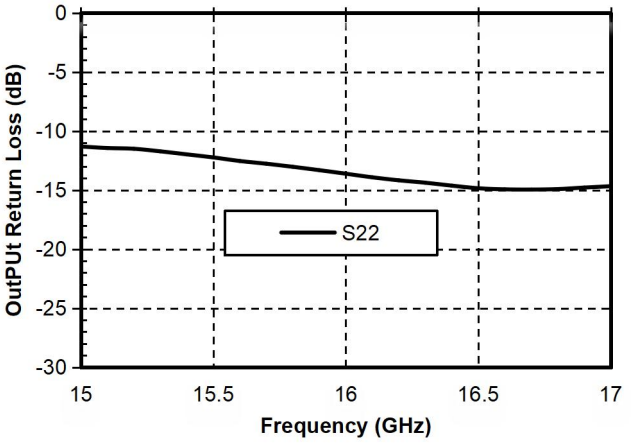

Reverse Isolation vs. Frequency



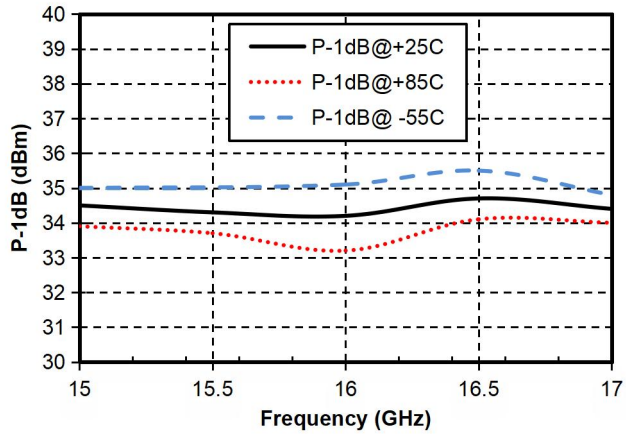

Input Return Loss vs. Frequency



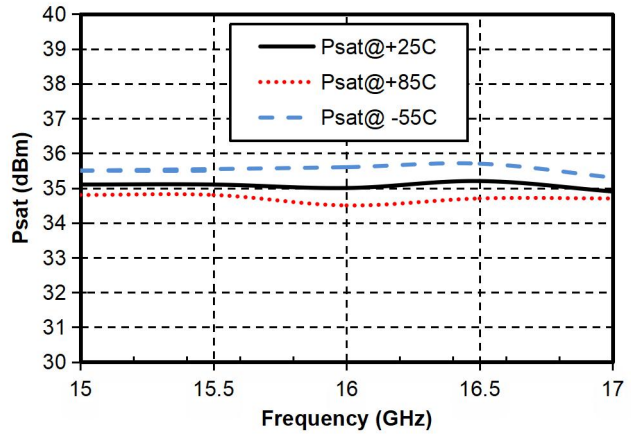

Output Return Loss vs. Frequency




P-1dB vs. Frequency




Psat vs. Frequency

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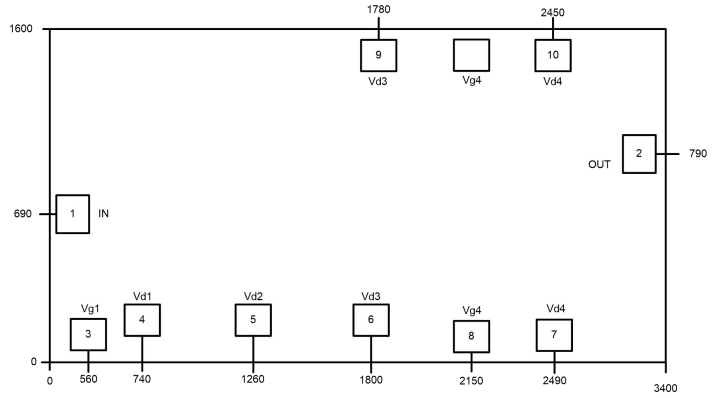
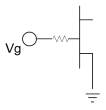
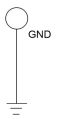
### Appearance structure [2]




【 2 】All units in the figure are micrometers

| Bonding point definition | | | |
|---|---|---|---|
| Bonding point number | Function Symbol | Functional Description | Equivalent Circuit |
| 1 | RF IN | The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.. |   |
| 2 | RF OUT | The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required. |   |
| 4, 5, 6, 7, 9, 10 | Vd 1~4 | Amplifier drain bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required. |   |
| 8 | Vg4 | Amplifier gate bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required. |   |
| Chip bottom | GND | needs to be in good contact with the RF and DC grounds. |   |

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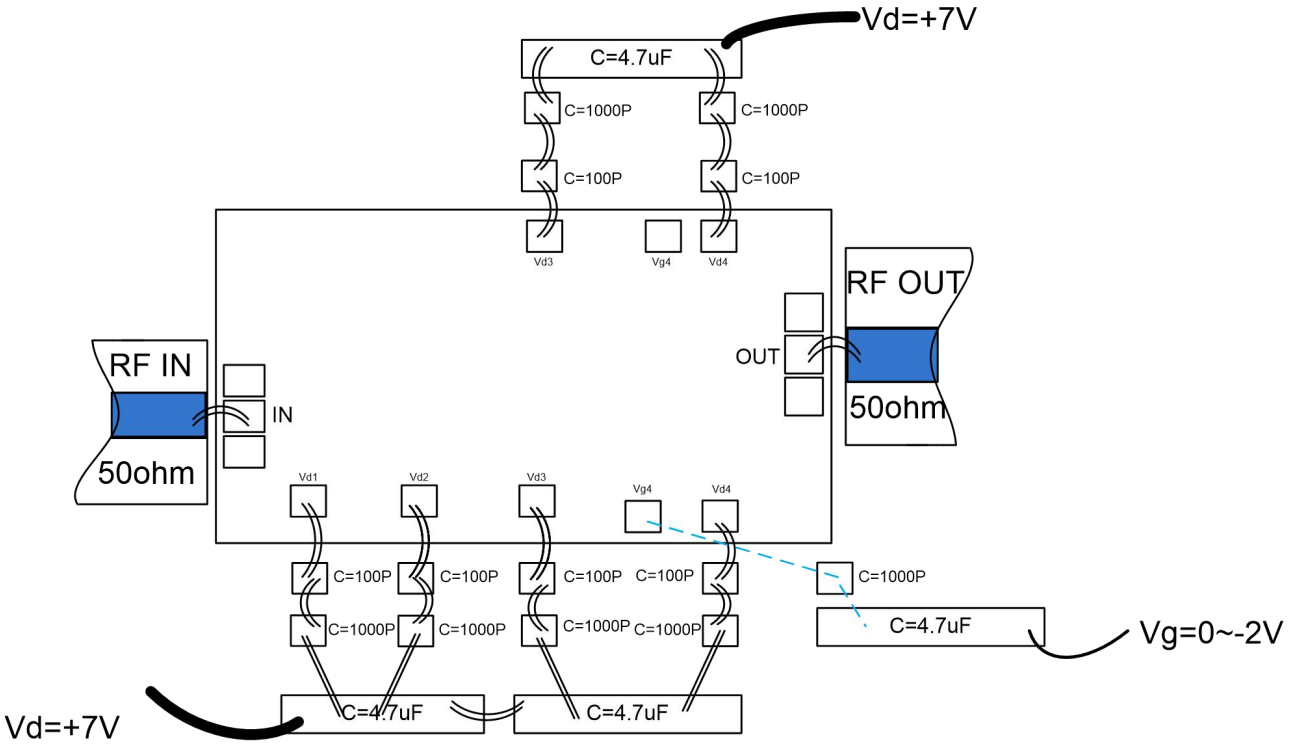
### Recommended assembly diagram




### Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting . The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding . Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).