

Performance characteristics

Frequency range: 13-15GHz Small Signal Gain: 26 dB

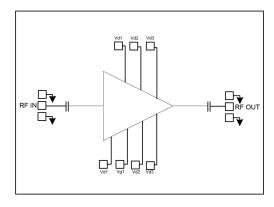
P -1dB: 37 dBm Psat: 37.5 dBm

OIP3: 42dBm@14GHz Power supply: 7 V/ 1300 mA

500hm input/output

Chip size: 3.24 x 3.12 x 0.1mm

Functional Block Diagram



Product Introduction

GPA -1315B is a high-gain, high- power amplifier chip based on GaAs technology, covering a frequency range of 13~15GHz, a small signal gain of 26dB, a P-1dB output power of 37dBm, and an additional efficiency of 33%. The chip via metallization process ensures good grounding, and the back side is metallized for eutectic sintering process.

Use restriction parameter ¹				
Maximum drain voltage	+8 V			
Maximum gate bias	- 3 V			
Maximum input power	+18 dBm			
Operating temperature	-55 ~ +85°C			
Storage temperature	-65 ~ +150°C			

[1] Exceeding any of these maximum limits may cause permanent damage.

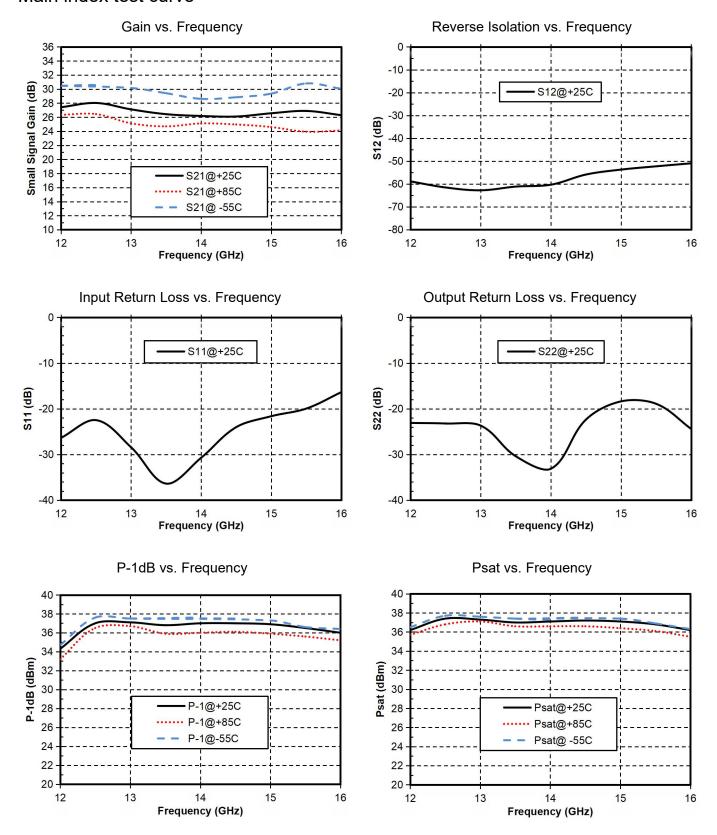
Electrical parameters (Ta=+25°C, Vd= 7 V, Ids= 1300 mA)					
index	Minimum	Typical Value	Maximum	unit	
Frequency Range	13 - 15			GHz	
Small Signal Gain	26	26	27	dB	
Gain Flatness	± 0.5			dB	
P-1dB	-	37	-	dBm	
Psat	37	37.5	-	dBm	
Input return loss	-	25	-	dB	
Output return loss	-	25	-	dB	
*5					

* By tuning the Vg terminal voltage -2V~0V, make lds reach 1300mA; the recommended gate voltage is -1.0V.

Tel: +65 82613258

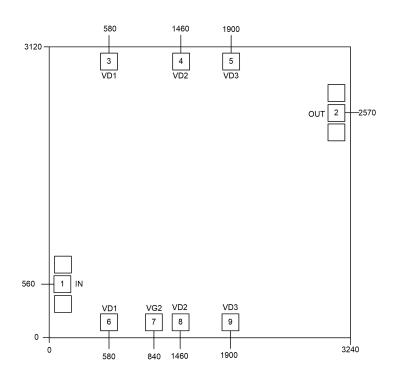


Main index test curve





Appearance structure ²

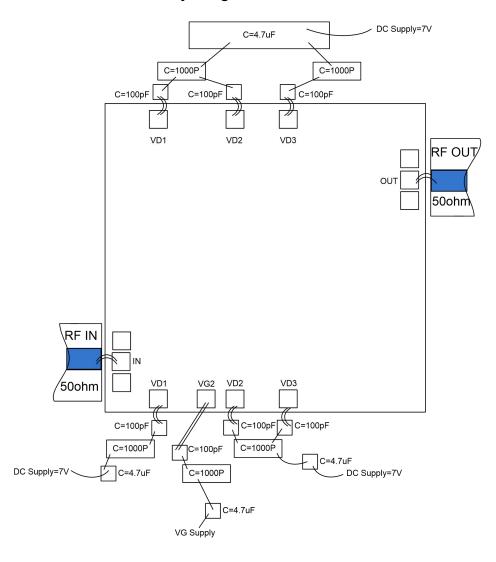


[2] All units in the figure are micrometers

Bonding point o	definition		
Bonding point number	Function Symbol	Functional Description	Equivalent Circuit
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.	RF IN
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.	RF OUT
3, 4, 5, 6, 8, 9	V D1~3	Amplifier drain bias, external 100pF, 1000pF, 4.7uF bypass capacitors are required.	Vdd
7	VG	Amplifier gate bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required.	V ₉ ○
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds	GND



Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip
 mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C. When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C. Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.





Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 °C. The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).

Add: 101 cecil street #14-10, tong eng building singapore 069533 Web: www.standardcircuit.com Tel: +65 82613258