

GaAs MMIC Power Amplifier Chip, 13-15GHz

Performance characteristics

Frequency range: 13-15GHz

Small Signal Gain: 28 dB

P -1dB: 32.5 dBm

Psat : 35 dBm

OIP3: 38dBm@14GHz

Power supply: 7 V/ 560 mA

50Ohm input/output

Chip size: 2.82 x 1.62 x 0.1mm

Product Introduction

GPA -1315A is a high-gain, high- power amplifier chip based on GaAs technology , covering a frequency range of 13~15GHz, a small signal gain of 28dB , a P -1dB output power of 32.5dBm, and an additional efficiency of 36% . The chip's via metallization process ensures good grounding, and the back side is metallized for eutectic sintering.

Use restriction parameter ¹

Maximum drain voltage	+8 V
Maximum gate bias	- 3 V
Maximum input power	+15 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd= 7 V, Ids= 560 mA)

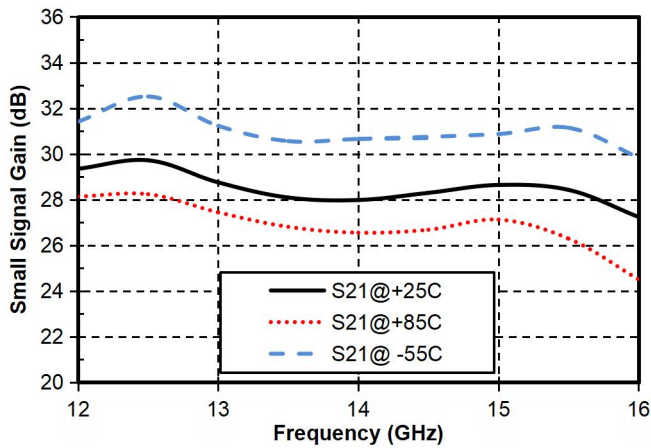
index	Minimum	Typical Value	Maximum	unit
Frequency Range	13 - 15			GHz
Small Signal Gain	-	28	-	dB
Gain Flatness	± 0.25			dB
P-1dB	-	32.5	-	dBm
Psat	-	35	-	dBm
Input return loss	-	18	-	dB
Output return loss	-	12	-	dB

* By tuning the Vg terminal voltage -2V~0V , make Ids reach 560mA; the recommended gate voltage is -1.0V.

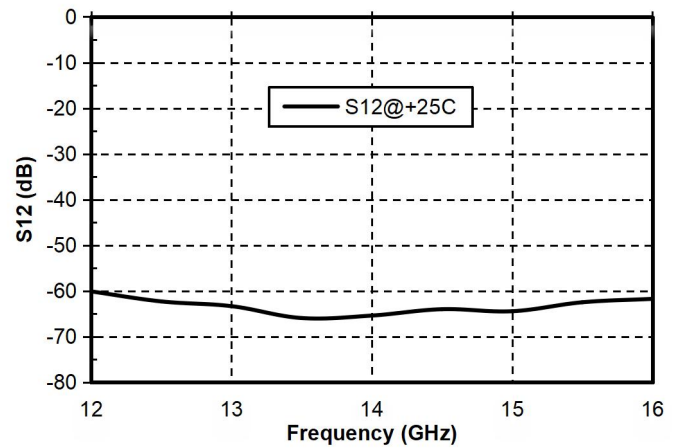
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Main index test curve

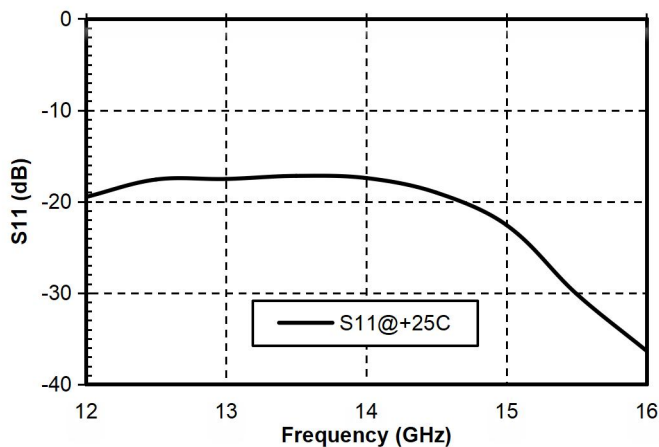
Gain vs. Frequency



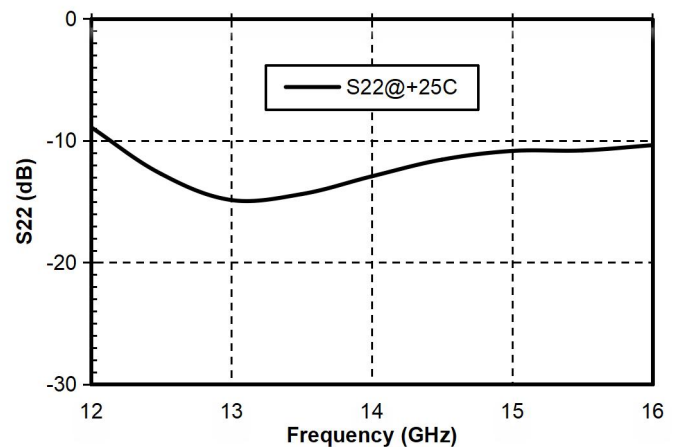
Reverse Isolation vs. Frequency



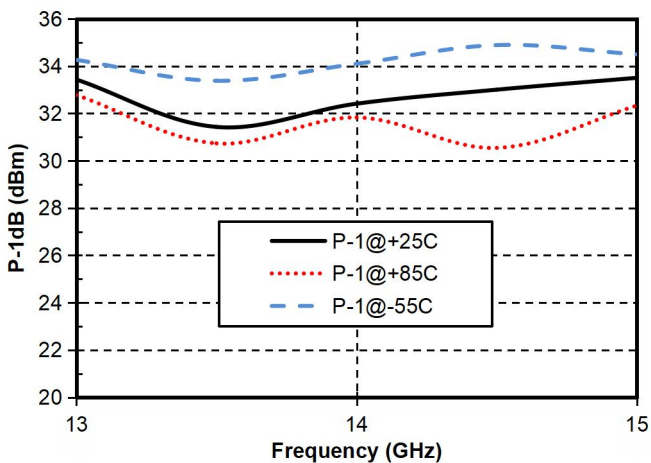
Input Return Loss vs. Frequency



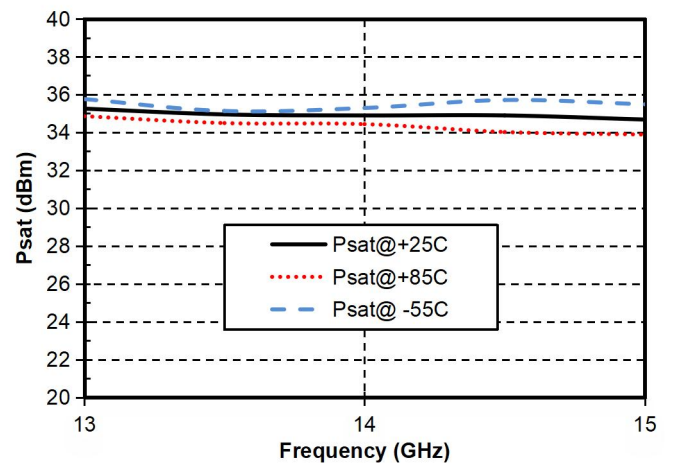
Output Return Loss vs. Frequency



P-1dB vs. Frequency

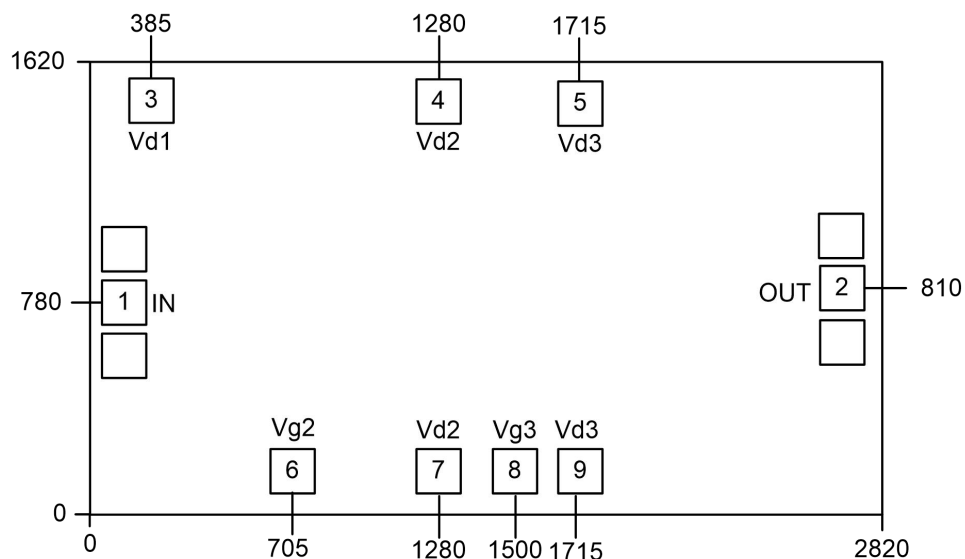


Psat vs. Frequency



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Appearance structure ²

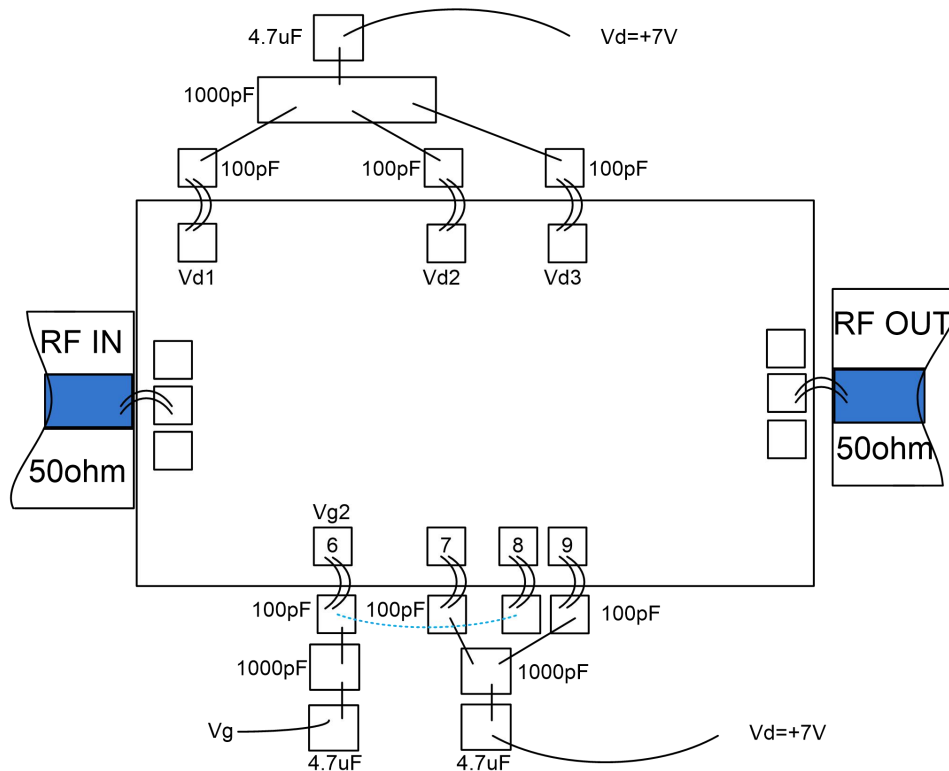


【 2 】 All units in the figure are micrometers

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
3, 4, 5, 7, 9	V D1~3	Amplifier drain bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required.
6, 8	VG2, VG3	Amplifier gate bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required.
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds.

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Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C . Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use $\Phi 0.025\text{mm}$ (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 °C . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).