GPA -1216D

GaAs MMIC Power Amplifier Chip, 12-16GHz

Performance characteristics

Frequency range: 12-16GHz
Small Signal Gain: 26 dB
P-1dB: 34.5 dBm
Psat: 35.5 dBm
OIP3: 40.5dBm@14GHz
Power supply: 7 V @1120 mA
50Ohm input/output
100% on-chip testing
Chip size: 3.06 x 2.0 x 0.1mm

Product Introduction

GPA -1216D is a broadband high-gain, high-linearity, high- power amplifier chip based on GaAs technology , covering a frequency range of 12~16GHz, a small signal gain of 26dB, and a Psat output power of 35.5dBm. The chip via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

Use restriction parameter [1]	
Maximum drain voltage	+9 V
Maximum gate bias	- 3 V
Maximum input power	+25 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd= +7 V, Vg=-1.0V, Ids= 1120 mA)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range		12-16		GHz
Small Signal Gain	25.5	26	26.5	dB
Gain Flatness		± 0.5		dB
P-1dB	-	34.5	-	dBm
Psat	-	35.5	-	dBm
OIP3@14GHz		40.5		dBm
Input return loss	9	11	-	dB
Output return loss	10.5	16	-	dB
Quiescent Current		1120		mA
* By tuning the Vg terminal voltage -2V~0V , the recommended gate voltage is -1.0V.				

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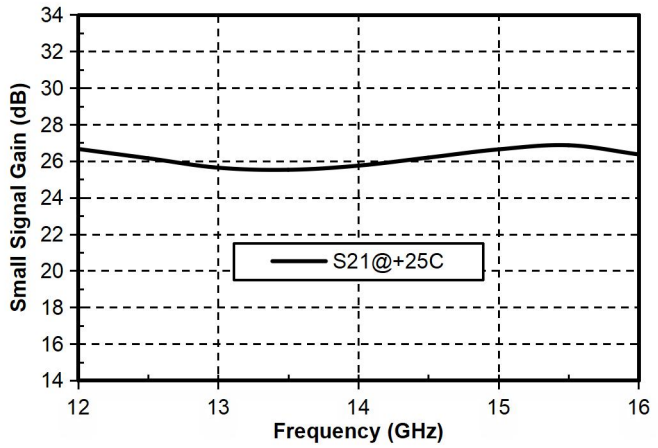
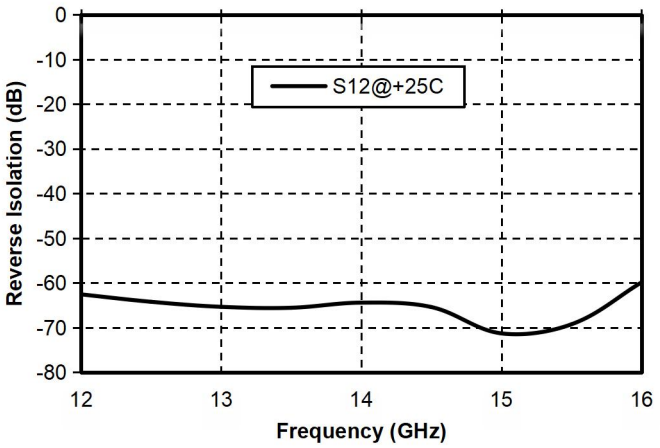
Main index test curve

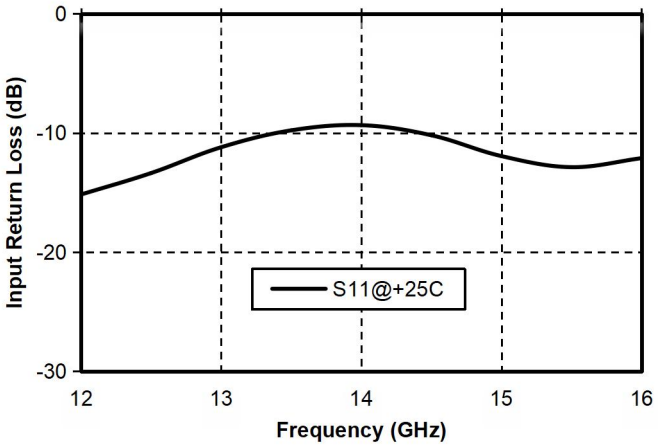
Gain vs. Frequency



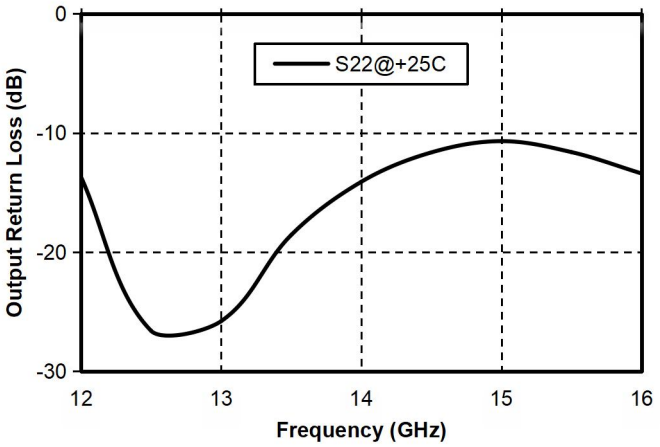
Reverse Isolation vs. Frequency



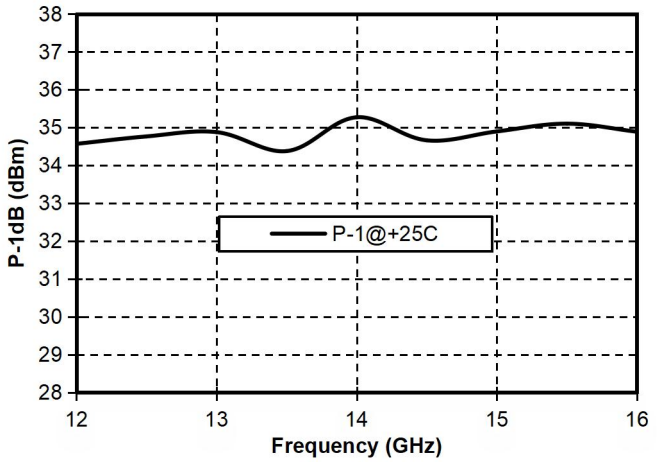
Input Return Loss vs. Frequency



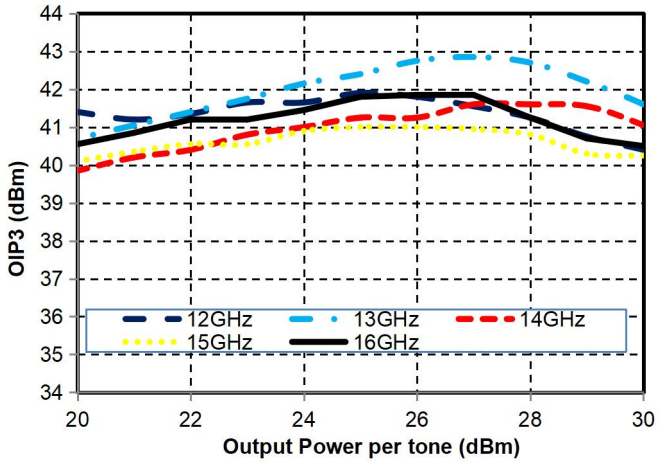
Output Return Loss vs. Frequency



P -1 vs. Frequency



OIP3 vs. Frequency



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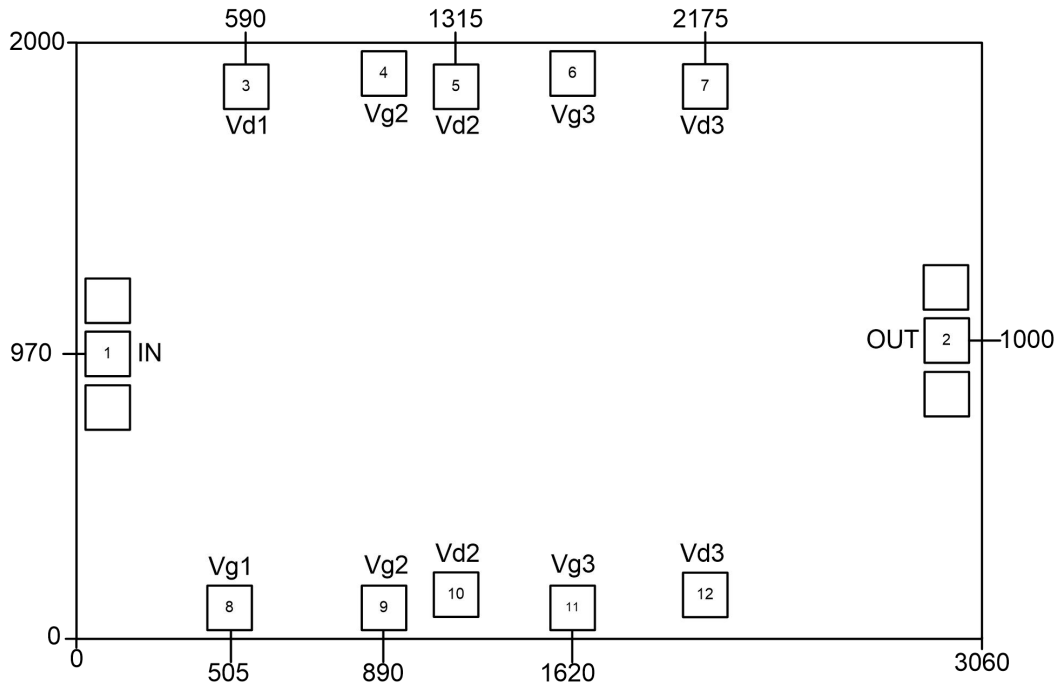
Appearance structure [2]



【 2 】All units in the figure are micrometers

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
3, 5, 7, 10, 12	V D1~4	Amplifier drain bias, external 50pF , 1000pF , 0.01uF, 4.7uF bypass capacitors are required.
4, 6, 8, 9, 11	VG1~2	Amplifier gate bias, external 50pF , 1000pF , 0.01uF, 4.7uF bypass capacitors are required.
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds.

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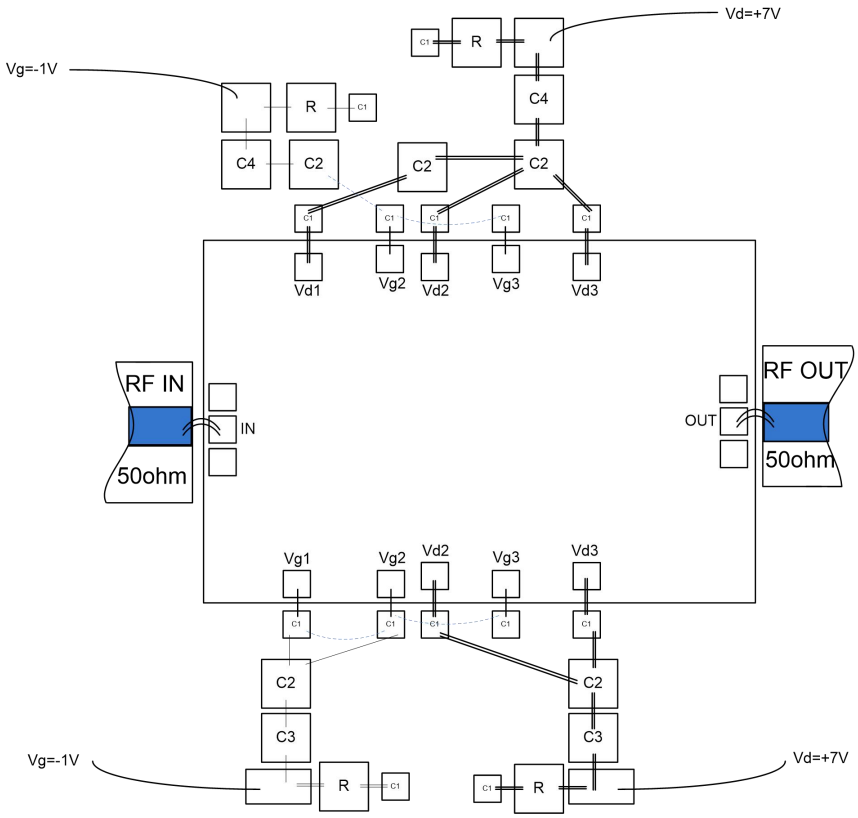
Recommended assembly drawing



raw material	Capacitance, inductance, resistance
C1	50pF
C 2	1000pF
C 3	0.01uF
R	10Ω

Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 ˚C and the tool (vacuum chuck) temperature reaches 265 ˚C . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ˚C . Do not let the chip exceed 320 ˚C for more than 20 seconds. The friction time should not exceed 3 seconds.

- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).

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