

Performance characteristics

Frequency range: 9-20GHz Small Signal Gain: 26 dB

P-1dB: 28 dBm @+5V, 29.5 dBm @+6V Psat: 28.5 dBm @+5V, 30 dBm @+6V

Power supply: +5 V / 520m A, +6 V / 470m A

500hm input/output

Chip size: 2.55 x 1.15 x 0.1mm

Use restriction parameter ¹

Maximum drain voltage +8 VMaximum gate bias -3 VMaximum input power +20 dBmOperating temperature $-55 \sim +85 ^{\circ}\text{C}$ storage temperature $-65 \sim +150 ^{\circ}\text{C}$

[1] Exceeding any of these maximum limits may cause

ermanent damage.

Product Introduction

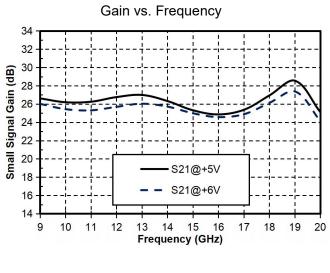
GPA -0920B is a broadband power amplifier chip based on GaAs technology, covering a frequency range of 9~20GHz, with a small signal gain of 26 dB and a P-1 output power of 28dBm. The chip can work at +6V, with a P-1 output power of 29.5dBm when working at +6V. The chip's via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

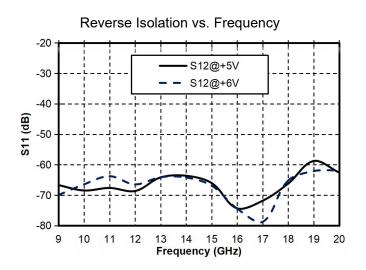
Electrical parameters (Ta=+25°C, Vd=+ 5 V, Ids= 520 mA)						
index	Minimum	Typical Value	Maximum	unit		
Frequency Range	9-20			GHz		
Small Signal Gain	25	26	28	dB		
Gain Flatness	± 1.5			dB		
P-1dB	26	28	-	dBm		
Psat	26.5	28.5	-	dBm		
Input return loss	-	17	-	dB		
Output return loss	-	15	-	dB		
* By tuning the Vg term	ninal voltage -2V~0V , th	e recommended gate volta	ge is -0.85V.			

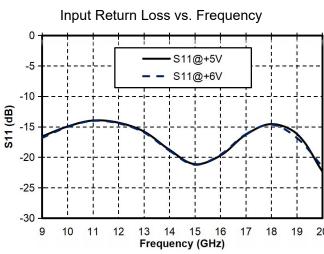
Electrical parameters (Ta=+25°C, Vd=+ 6 V, Ids= 470 mA)					
Frequency Range		9-20		GHz	
Small Signal Gain	24	25.5	27	dB	
Gain Flatness	± 1.5			dB	
P-1dB	28.5	29.5	-	dBm	
Psat	29	30	-	dBm	
Input return loss	-	17	-	dB	
Output return loss	-	15	-	dB	
* By tuning the Vg tern	ninal voltage -2V~0V , t	he recommended gate volta	age is -0.9V.		

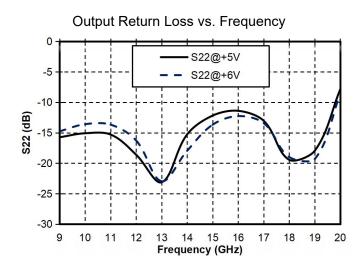


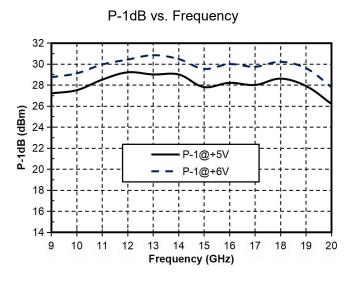
Main index test curve

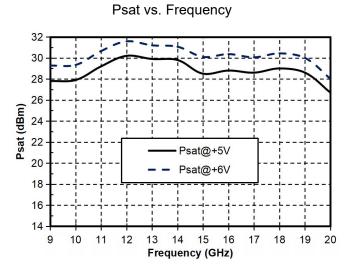






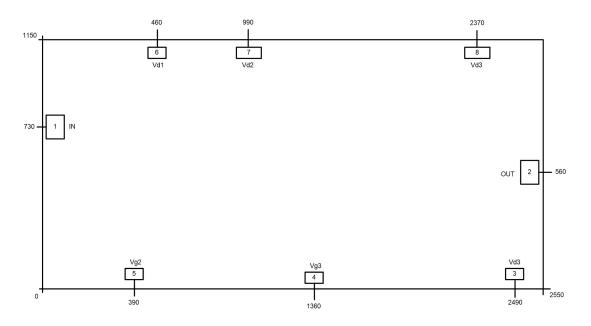








Appearance structure ²

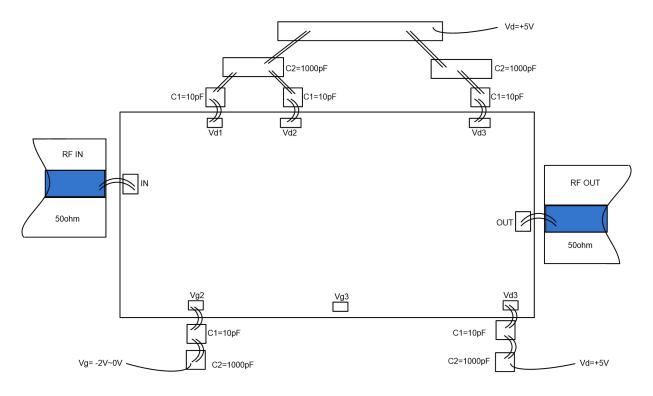


[2] All units in the figure are micrometers

Bonding point definition					
Bonding point number	Function Symbol	Functional Description			
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required			
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required			
3, 6, 7, 8	V D1~3	Amplifier drain bias, requires external 10 pF, 1000 pF, 100 nF bypass capacitor			
4, 5	VG	Amplifier gate bias, external 10 pF, 1000 pF, 100 nF bypass capacitor required			
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds			



Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip
 mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C. When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C. Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 °C. The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).