

GaAs MMIC Power Amplifier Chip, 8-12GHz

Performance characteristics

Frequency range: 8-12GHz
 Small Signal Gain: 16.5 dB
 P-1dB: 31.5 dBm
 Psat: 32 dBm
 PAE : 42%
 Power supply: +8V / 200mA
 50Ohm input/output
 100% on-chip testing
 Chip size: 2.05 x 1.5 x 0.1mm

Product Introduction

GPA-0812B is a broadband high-gain, high-efficiency, high- power amplifier chip based on GaAs technology , covering a frequency range of 8~12GHz, a small signal gain of 16.5dB, a P-1 output power of 31.5dBm , and a saturation efficiency of 40% . The chip via metallization process ensures good grounding, and the back side is metallized for eutectic sintering process.

Use restriction parameter ¹	
Maximum drain voltage	+10 V
Maximum gate bias	-3 V
Maximum input power	+20 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

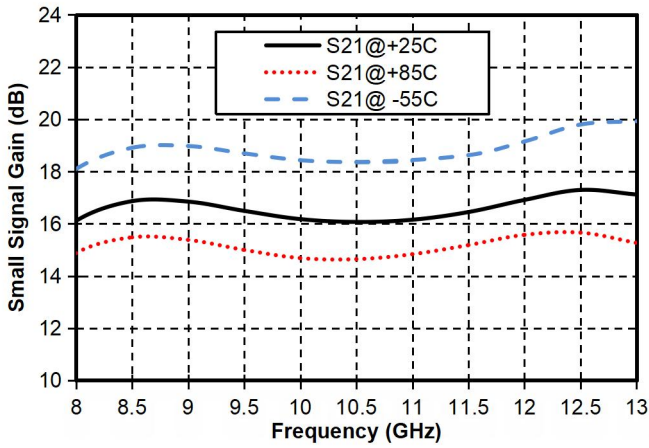
Electrical parameters (Ta=+25°C, Vd =+ 8 V, Ids= 200 mA)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	8 - 12			GHz
Small Signal Gain	16	16.5	17	dB
Gain Flatness	± 0.5			dB
Reverse Isolation		51		dB
P-1dB	31	31.5	-	dBm
Psat	31.5	32	-	dBm
PAE	37	42	-	%
Noise	-	6.5	-	
Input return loss	14	15	-	dB
Output return loss	9.5	11	-	dB

* By tuning the Vg terminal voltage -2V~0V , the recommended gate voltage is -0.85V.

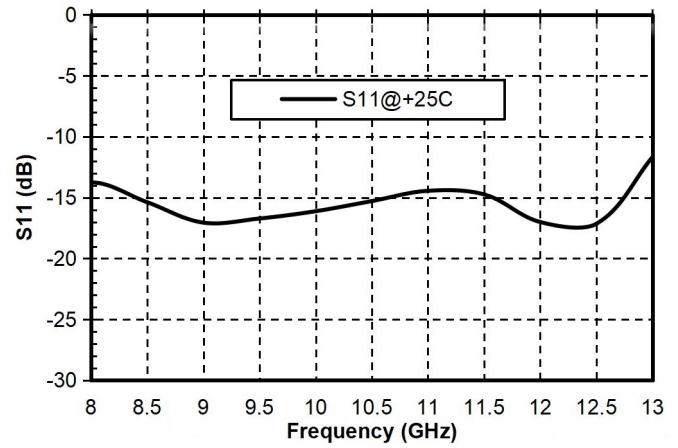
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Main index test curve

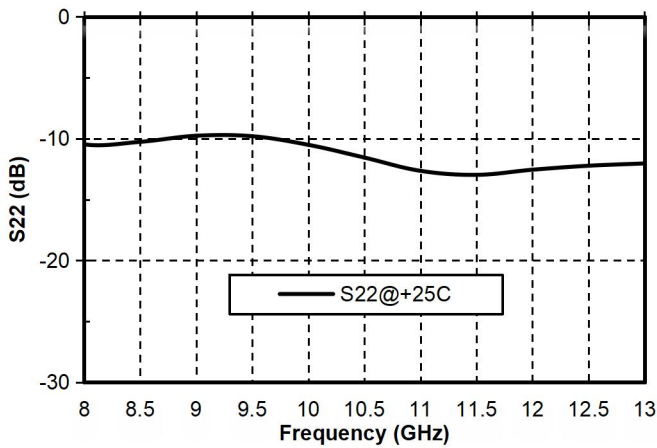
Gain vs. Frequency



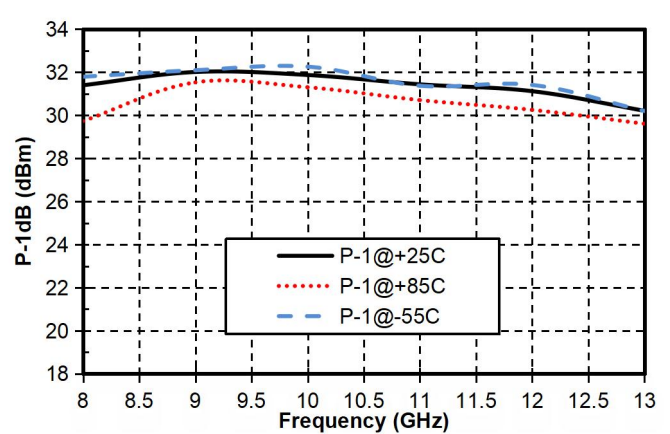
Input Return Loss vs. Frequency



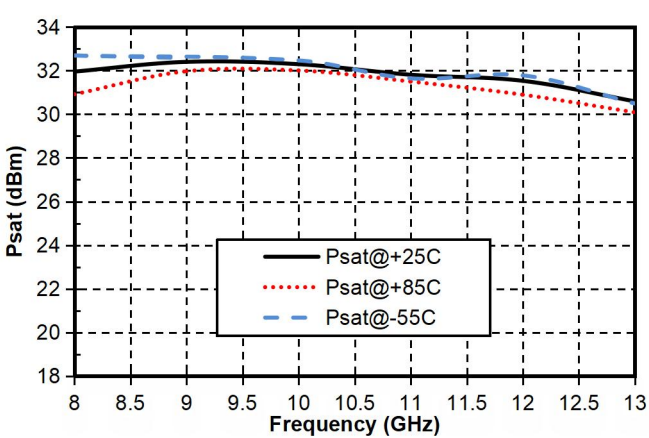
Output Return Loss vs. Frequency



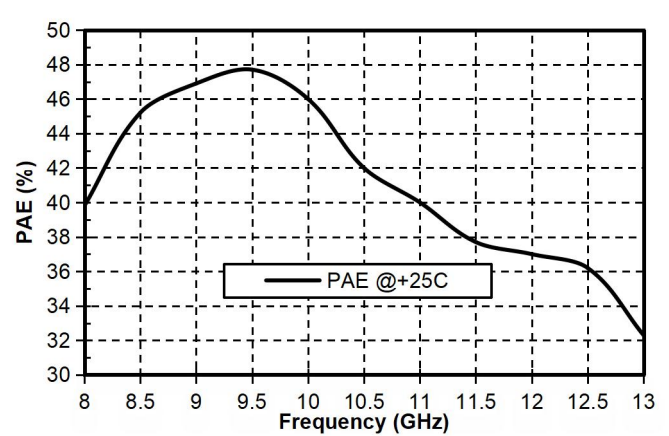
P-1dB vs. Frequency



Psat vs. Frequency

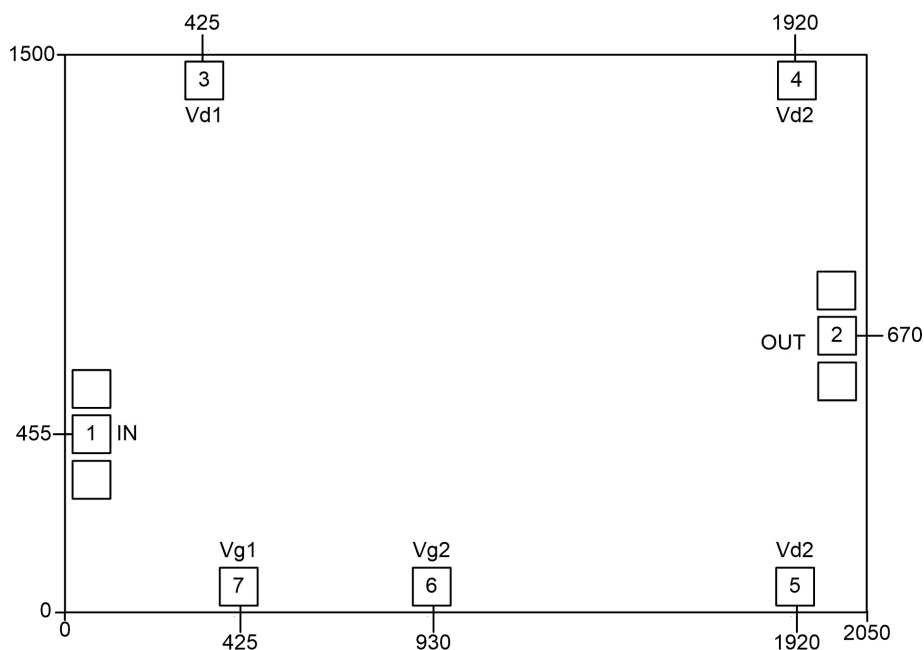


PAE vs. Frequency



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Appearance structure ²

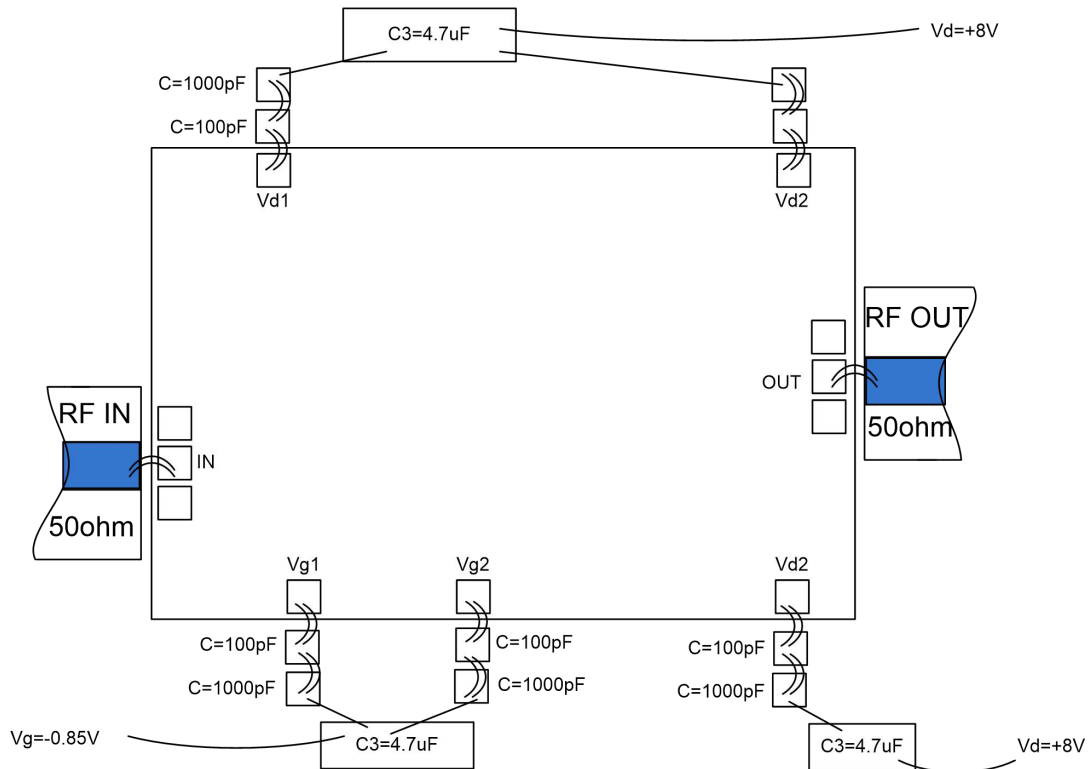


【 2 】 All units in the figure are micrometers

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
3, 4, 5	V D1~2	Amplifier drain bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required.
6, 7	VG	Amplifier gate bias, external 100pF , 1000pF , 4.7uF bypass capacitors are required.
Chip bottom	GND	needs to be in good contact with the RF and DC grounds.

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Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting . The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C . Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use $\Phi 0.025\text{mm}$ (1mil) gold wire for both ball and wedge bonding . Thermosonic bonding temperature is 150 °C . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).