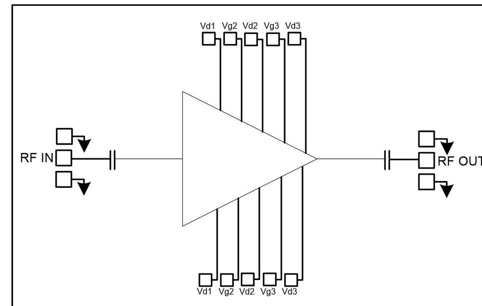
GaAs MMIC Power Amplifier Chip, 6-18GHz

Performance characteristics

Frequency range: 6-18GHz
Small signal gain: 26 dB@ +5V, 25dB@+6V
P-1dB: 30.5dBm@+5V , 32dBm@+6V
Psat : 31dBm @ +5V, 32.5dBm@+6V
Power supply: +5V@1100mA, + 6V @ 1100mA
50Ohm input/output
100% on-chip testing
Chip size: 3.3 x 2.4 x 0.1mm

Functional Block Diagram



Product Introduction

GPA -0618E is a broadband high-gain, high-efficiency, high- power amplifier chip based on GaAs technology , covering a frequency range of 6~18GHz, with a small signal gain of 26 dB and a Psat output power of 31 dBm when operating at +5V; and a small signal gain of 25dB and a Psat output power of 32.5dBm when operating at +6V. The chip's via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering process.

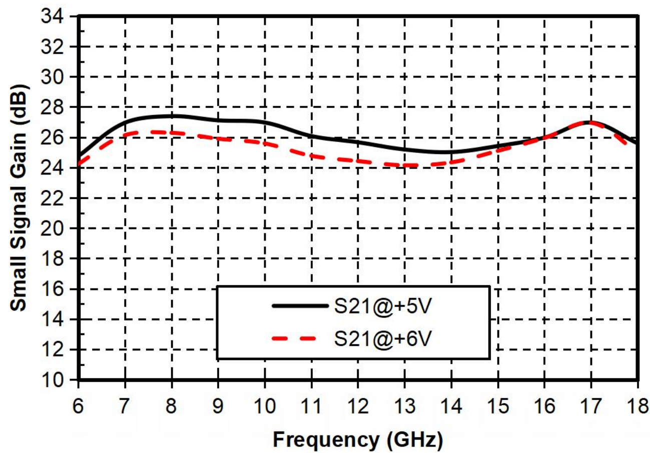
Use restriction parameter [1]	
Maximum drain voltage	+9 V
Maximum gate bias	- 3 V
Maximum input power	+25 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

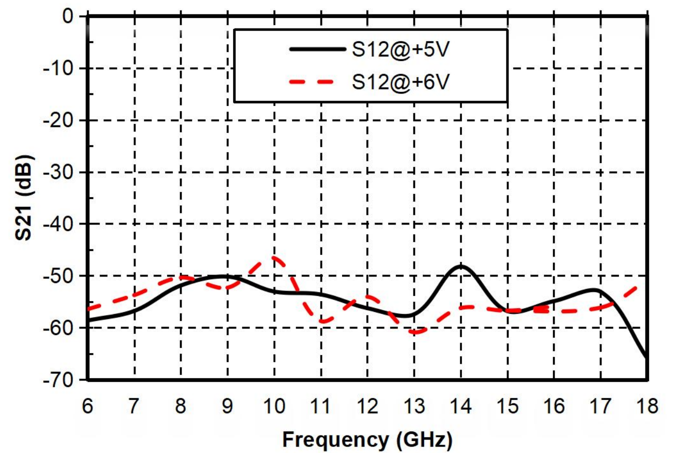
Electrical parameters (Ta=+25°C, Vd= +5 V, Vg=-0.75V, Ids= 1100 mA)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range	6-18			GHz
Small Signal Gain	-	26	-	dB
Gain Flatness	± 1.3			dB
P-1dB	-	30.5	-	dBm
Psat	-	31	-	dBm
Input return loss	-	15	-	dB
Output return loss	-	20	-	dB
* By tuning the Vg terminal voltage -2V~0V , the recommended gate voltage is -0.75V.				

Main index test curve

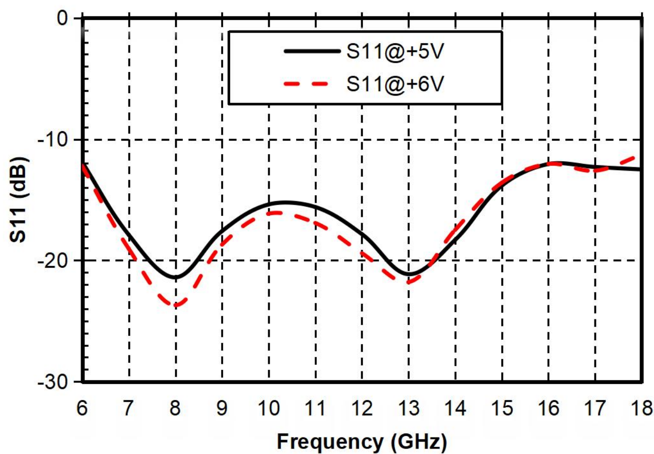
Gain vs. Frequency



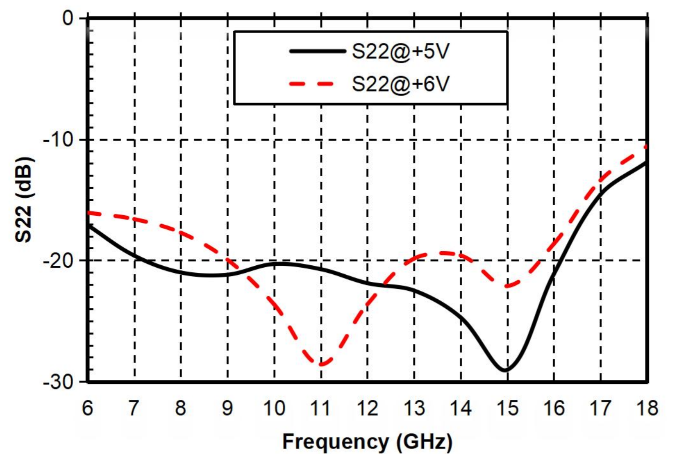
Reverse Isolation vs. Frequency



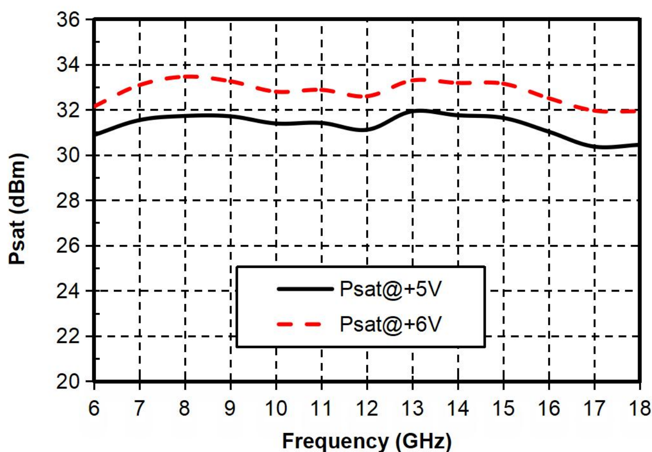
Input Return Loss vs. Frequency



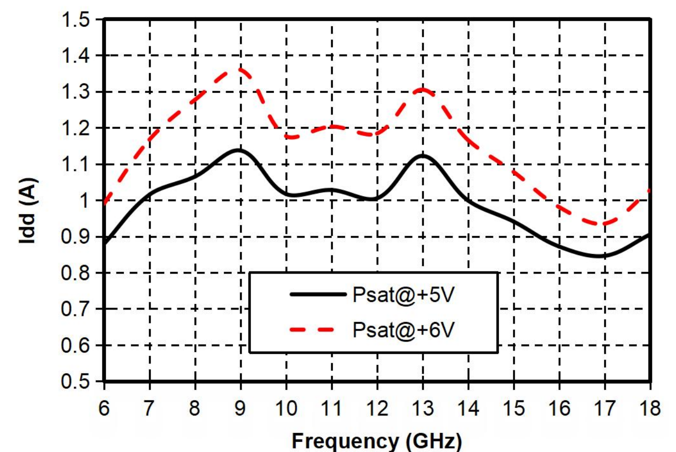
Output Return Loss vs. Frequency



P- sat vs. frequency



Dynamic Current vs. Frequency



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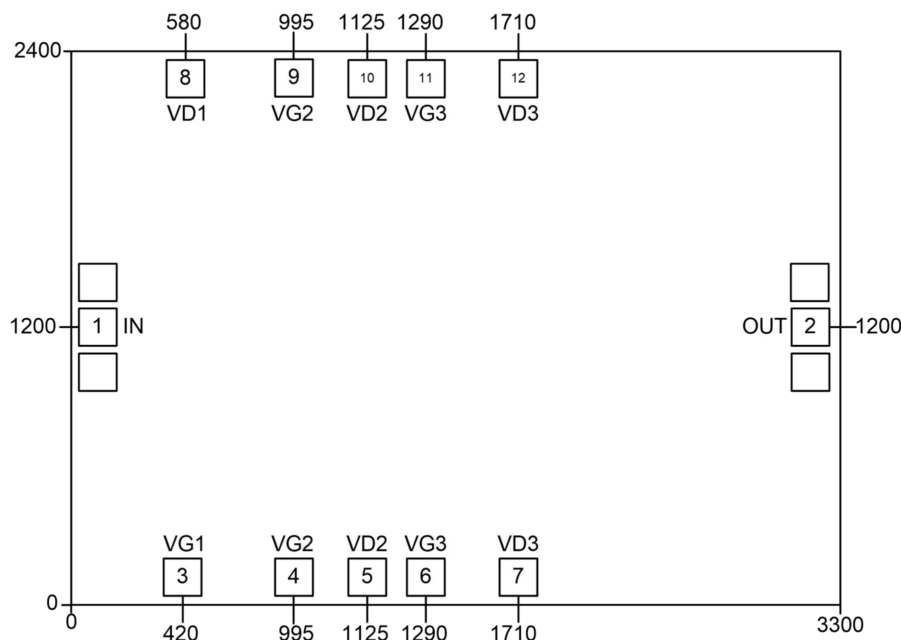
Appearance structure [2]



【 2 】The units in the figure are all micrometers (dimensional tolerance: ±100um.)

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required.
5, 7, 8, 10, 12	V D1~3	Amplifier drain bias, external 100pF , 1000pF bypass capacitors are required.
3, 4, 6, 9, 11	VG1~3	Amplifier gate bias, external 100pF , 1000pF bypass capacitors are required.
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds.

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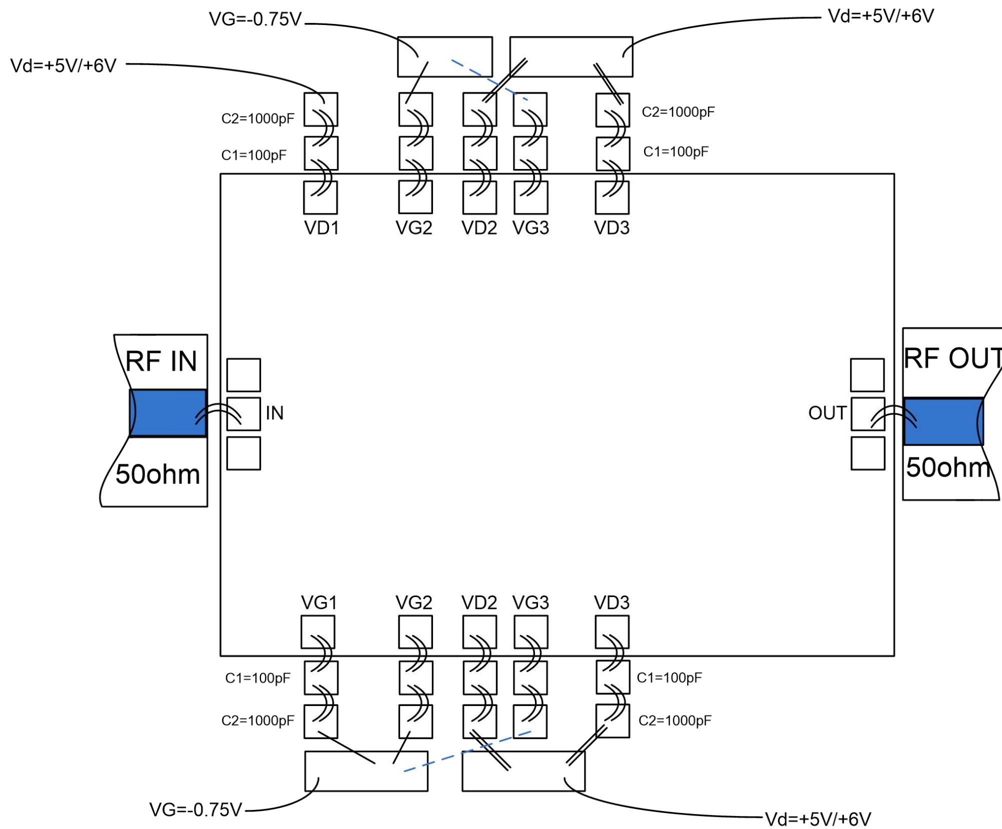
Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).