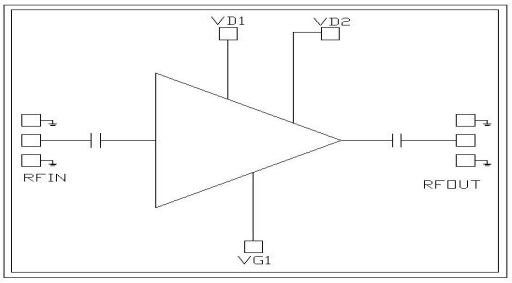
GPA-0618-26

GaAs MMIC Power Amplifier Chip, 6-18GHz

Performance characteristics

Frequency range: 6-18GHz
Small Signal Gain: 18 dB
Noise figure: 8dB
P-1dB：24. 5dBm
Psat: 26dBm
Power supply: +7V/290mA
50Ohm input/output
100% on-chip testing
Chip size: 1.35 x 1.025 x 0.1 mm

Functional Block Diagram



Product Introduction

GPA-0618-26 is a broadband high dynamic, low noise, medium power amplifier chip based on GaAs process , with a frequency range of 6GHz~18GHz, a small signal gain of 18dB , and a saturated output power of 26dBm. The chip via metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding process.

Use restriction parameter [1]	
Maximum drain voltage	+9V
Maximum gate bias	-3V
Maximum input power	+15dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (TA = +25°C, Vd = +7V)				
index	Minimum	Typical Value	Maximum	unit
Frequency Range		6-18		GHz
Small Signal Gain	16	1 8	1 9	dB
Gain Flatness	-	±1.0	-	dB
Noise Figure		8.0	-	
P-1dB	21	24.5	26	dBm
Psat	23	27	26.5	dBm
Input return loss		20		dB
Output return loss		8		dB
Quiescent Current		290		mA
By adjusting the Vg terminal voltage from -2V to 0V, 290mA can be achieved.				

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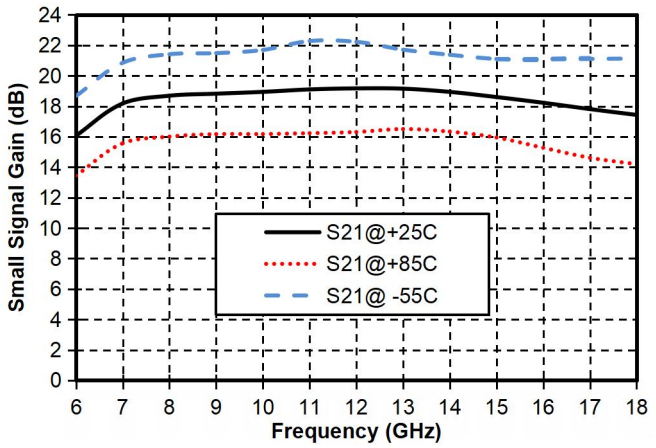
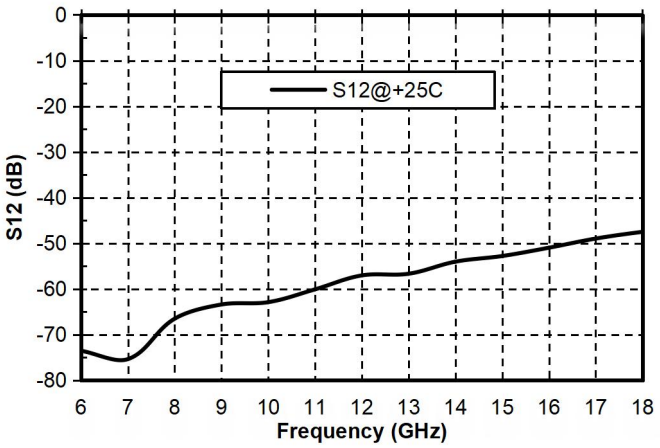
Main index test curve

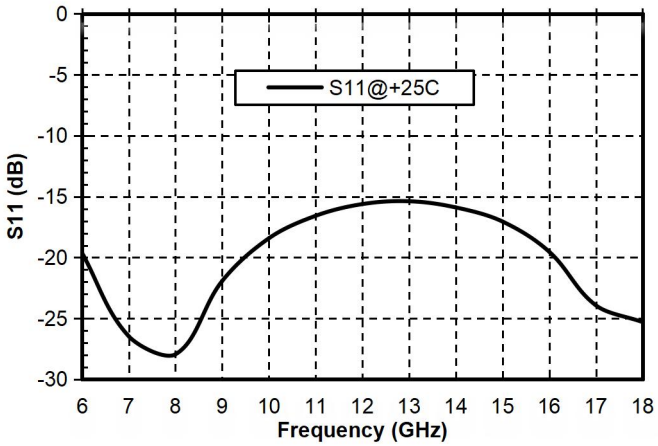
Gain vs. Frequency



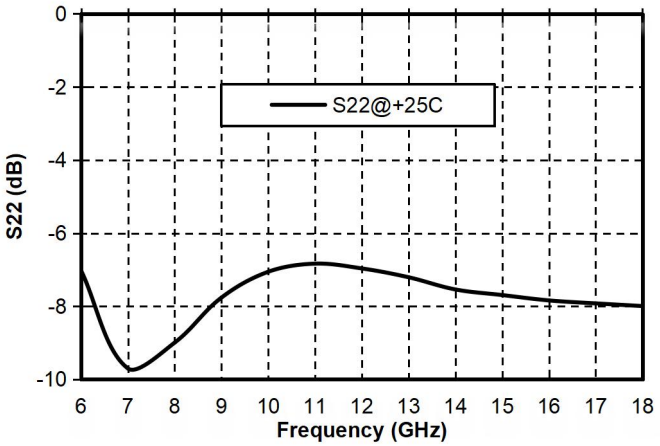
Reverse Isolation vs. Frequency



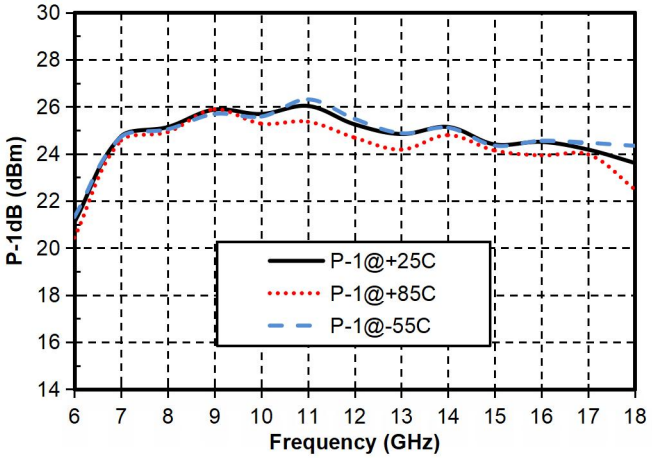
Input Return Loss vs. Frequency



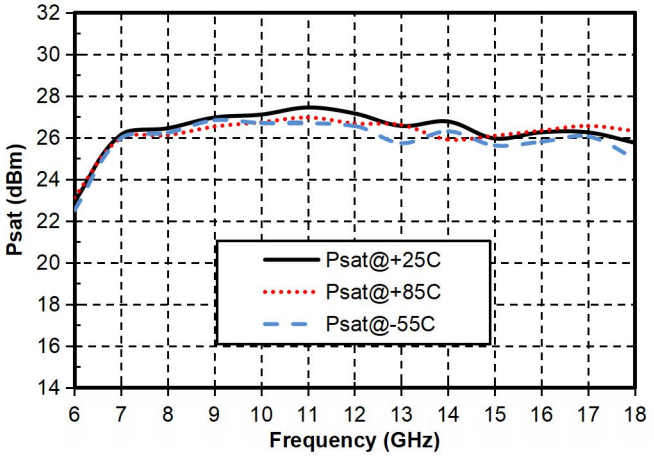
Output Return Loss vs. Frequency



P-1dB vs. Frequency



Psat vs. Frequency



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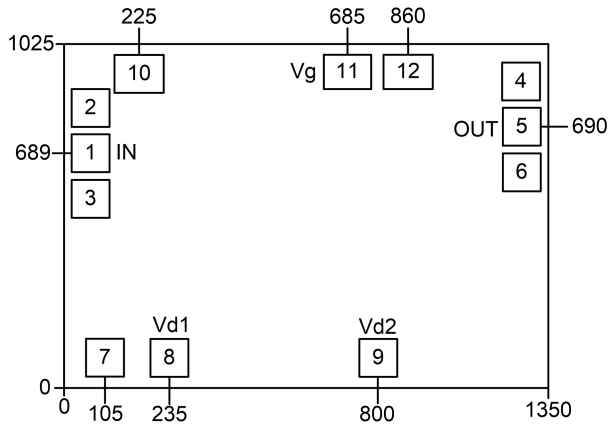
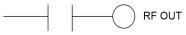
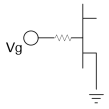
Appearance structure [2]



【 2 】All units in the figure are micrometers

Bonding point definition			
Bonding point number	Function Symbol	Functional Description	Equivalent Circuit
1	RFIN	RF signal input terminal, no DC blocking capacitor required.	
5	RFOUT	RF signal output terminal, no DC blocking capacitor required.	
8	Vd1	Amplifier drain bias, requires external 100pF bypass capacitor.	
9	Vd2	Amplifier drain bias, requires external 100pF bypass capacitor.	
11	Vg	Amplifier gate bias, requires external 100pF bypass capacitor.	
2, 3, 4, 6, 10, 12	GND	Ground pressure point for probe testing.	
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC.	

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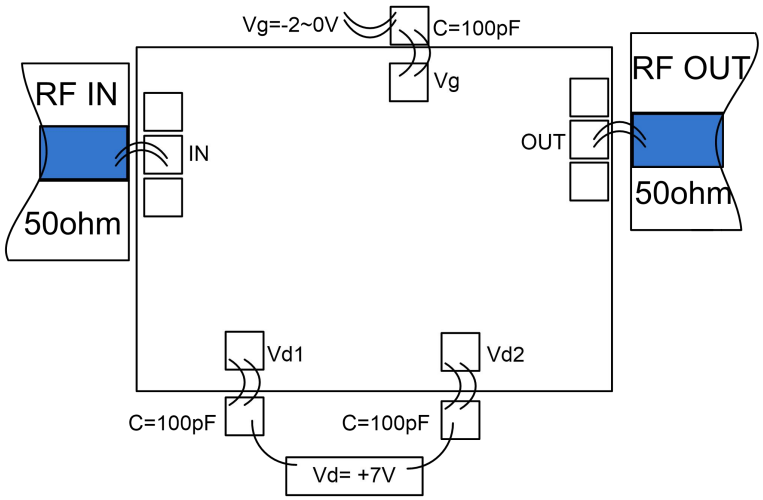
Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position, the conductive glue can be vaguely seen around it. For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).