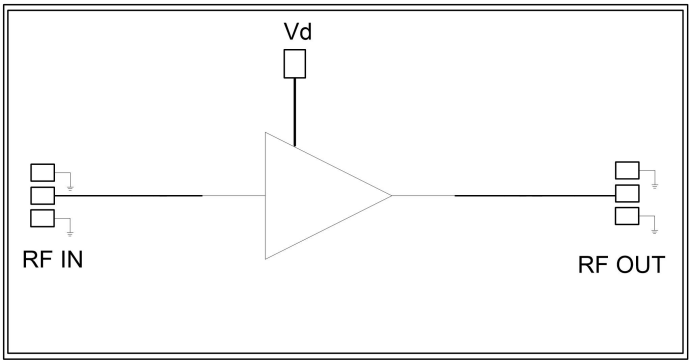
GPA-0218-28

GaAs MMIC Power Amplifier Chip, 2-18GHz

Performance characteristics

Frequency range: 2-18GHz
Small signal gain: 13dB
P-1dB: 27.5dBm
Psat: 28.5dBm
Power supply: +10 V/ 350 mA
50Ohm input/output
100% on-chip testing
Chip size: 2.5 x 1.65 x 0.1mm

Functional Block Diagram



Product Introduction

GPA -0218-28 is an ultra-wideband distributed amplifier chip based on pHEMT process, covering the frequency range of 2~18GHz, small signal gain of 13dB, and saturated output power of 28.5dBm. GPA-0218-28 is powered by a single +10V power supply. The chip through-hole metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding process.

Use restriction parameter [1]	
Maximum drain voltage	+14V
Maximum gate bias	-3V
Maximum input power	+2 3 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd= +10 V, Ids= 350 mA)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	2 -18			GHz
Small Signal Gain	9.5	13	15.5	dB
Gain Flatness	± 3			dB
P-1dB	26.5	27.5	28.5	dBm
Psat	27.5	28.5	29.5	dBm
Input return loss	15	18	-	dB
Output return loss	10	12	-	dB
Thermal resistance	Substrate temperature +85 ˚C , RF signal input, Rth=18.5 ˚C /W			

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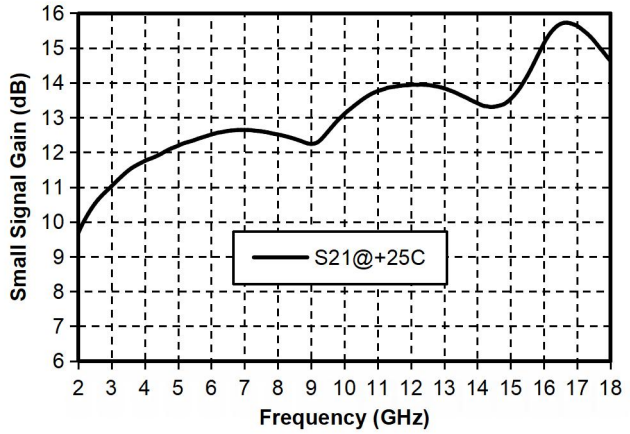
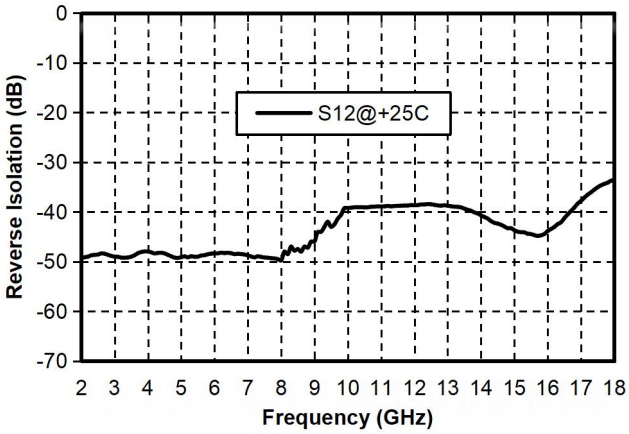
Main index test curve

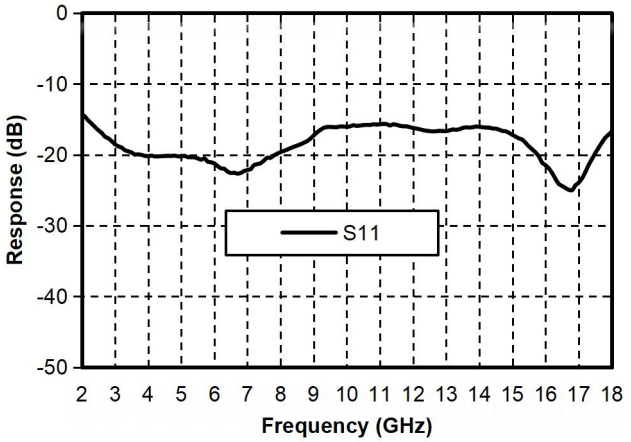
Gain vs. Frequency



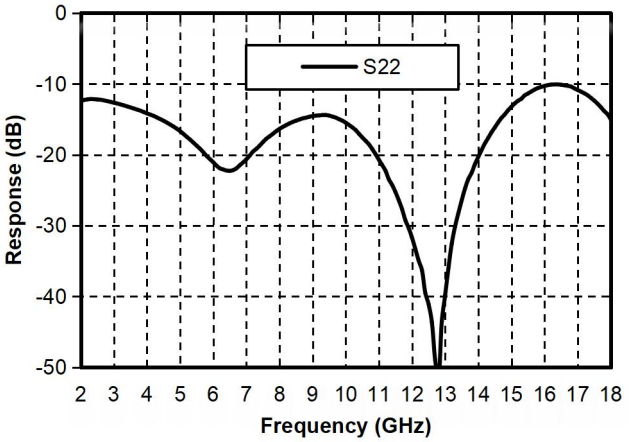
Reverse Isolation vs. Frequency



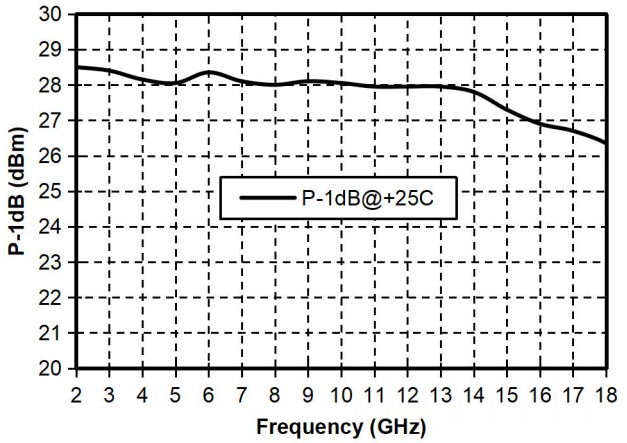
Input Return Loss vs. Frequency



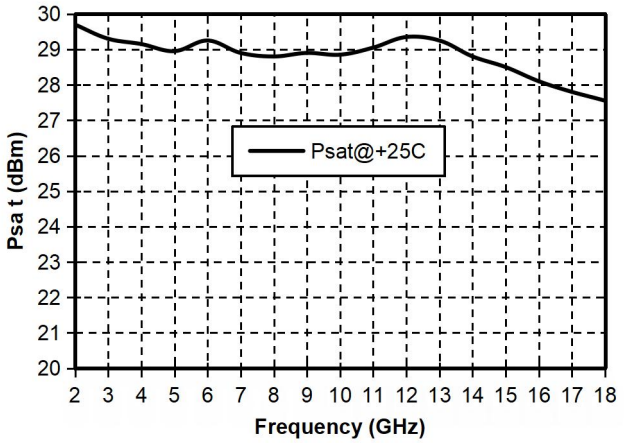
Output Return Loss vs. Frequency



P-1dB vs. Frequency



Psat vs. Frequency



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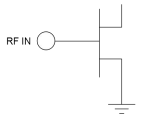
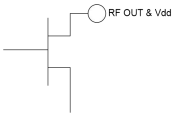
Appearance structure [2]

【2】The units in the figure are all micrometers (dimensional tolerance: ±50um.)

Bonding point definition

Bonding point number	Function Symbol	Functional Description	Equivalent Circuit
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required	
2	RF OUT	The signal output terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required	
3	Vd	Amplifier drain bias, requires external broadband inductor and 100pF bypass capacitor	
Chip bottom	GND	The bottom of the chip needs to be in good contact with the RF and DC grounds	

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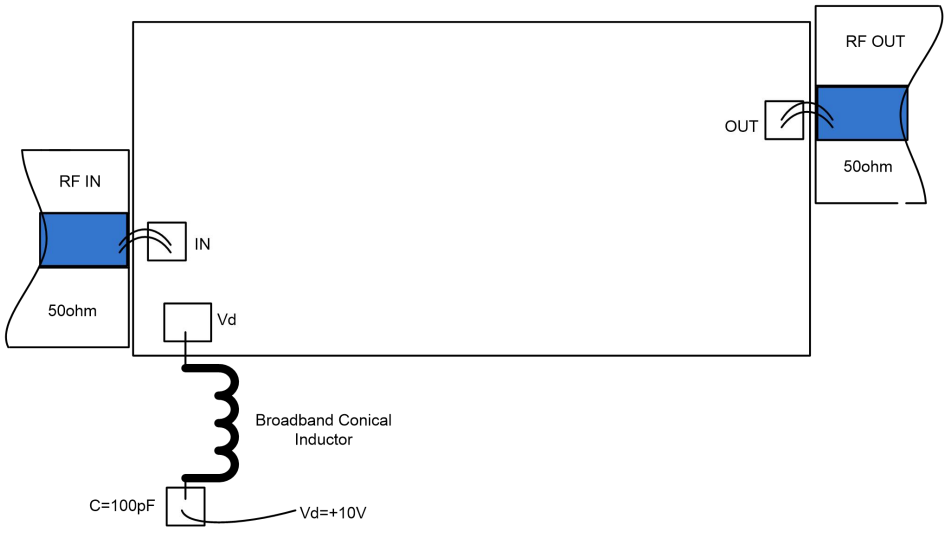
Recommended assembly diagram



Notice

- The chip should be stored in an anti-static container and in a nitrogen environment. It should be stored in an environment with a temperature of 10℃~30℃ and a relative humidity of less than 30%.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20. The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position, the conductive glue can be vaguely seen around it. For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding. Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding. Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).