

GaAs MMIC Power Amplifier Chip, 2.6- 4.2GHz

Performance characteristics

Frequency range: 2.6-4.2 GHz

Small Signal Gain: 26 dB

P-1dB: 24 dBm

Psat: 25 dBm

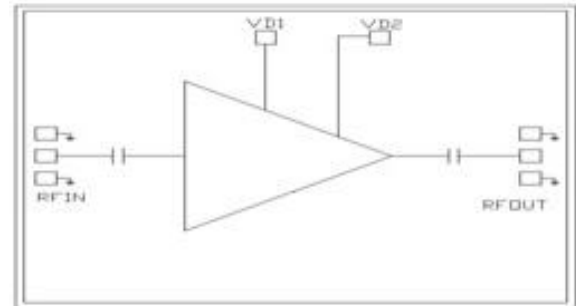
Power supply: +5 V / 140 mA

50Ohm input/output

100% on-chip testing

Chip size : 2.72 x 1.6 x 0.1 mm

Functional Block Diagram



Product Introduction

GPA-0204C is a broadband power amplifier chip based on GaAs technology, with a frequency range of 2.6 GHz~4.2 GHz, a small signal gain of 26dB, and a saturated output power of 25dBm. GPA-0204A is powered by a single +5V power supply. The chip through-hole metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding process.

Use restriction parameter ¹

Maximum drain voltage	+7 V
Maximum input power	+20 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

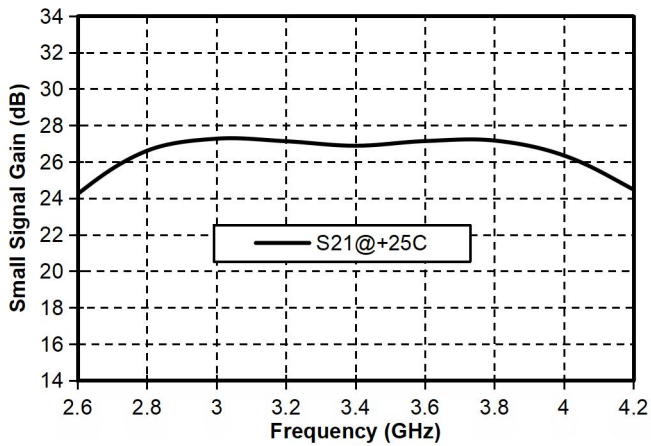
Electrical Parameters (TA = +25°C, Vd = +5 V)

Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	2.6 - 4.2			GHz
Small Signal Gain	-	26	-	dB
Gain Flatness	-	± 1 . 5	-	dB
P-1dB	-	24	-	dBm
Psat	-	25	-	dBm
Input return loss	-	14	-	dB
Output return loss	-	19	-	dB
Quiescent Current	-	140	-	mA

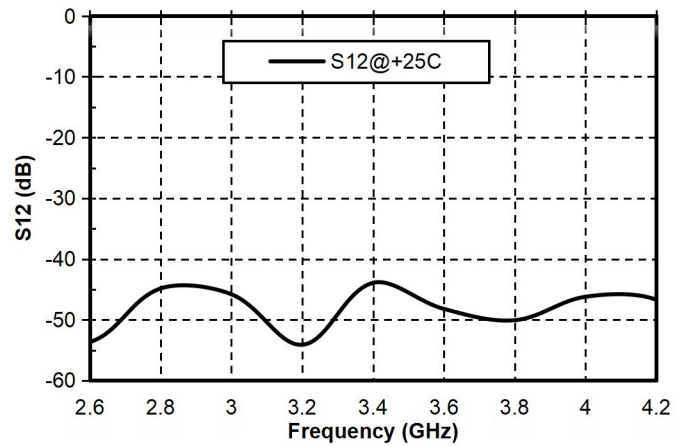
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Main index test curve

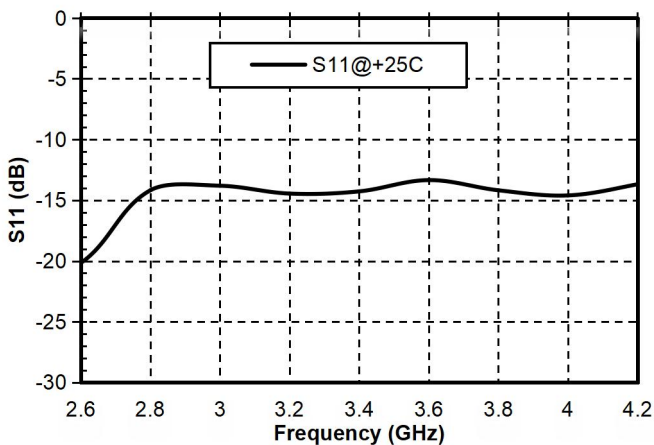
Gain vs. Frequency



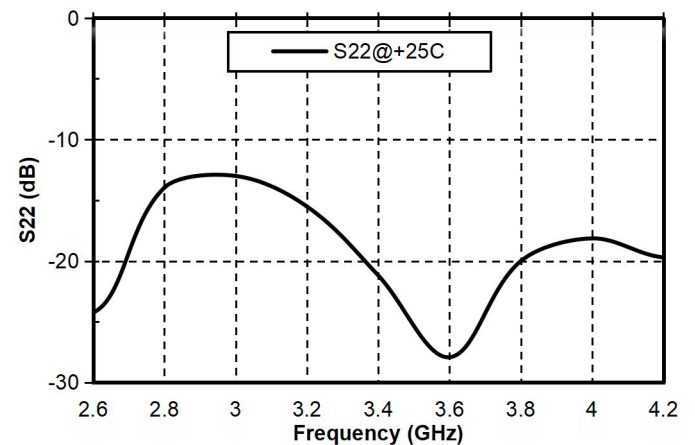
Reverse Isolation vs. Frequency



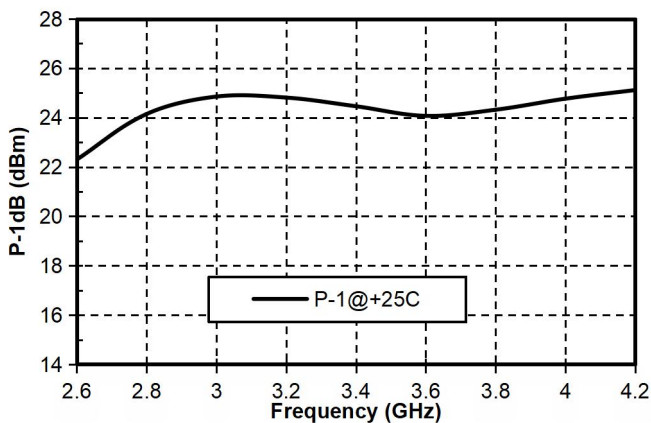
Input Return Loss vs. Frequency



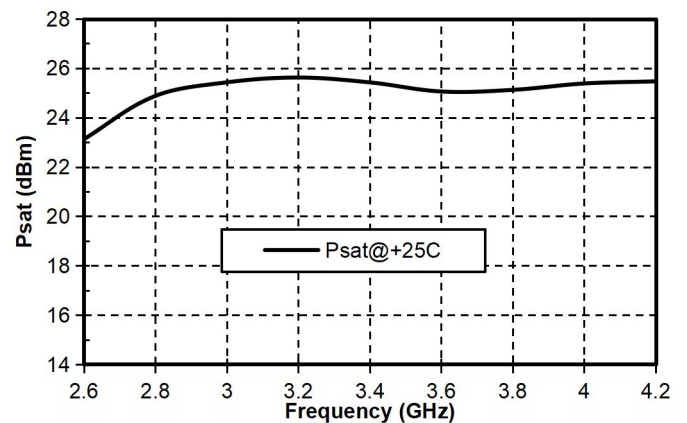
Output Return Loss vs. Frequency



P-1 vs. Frequency

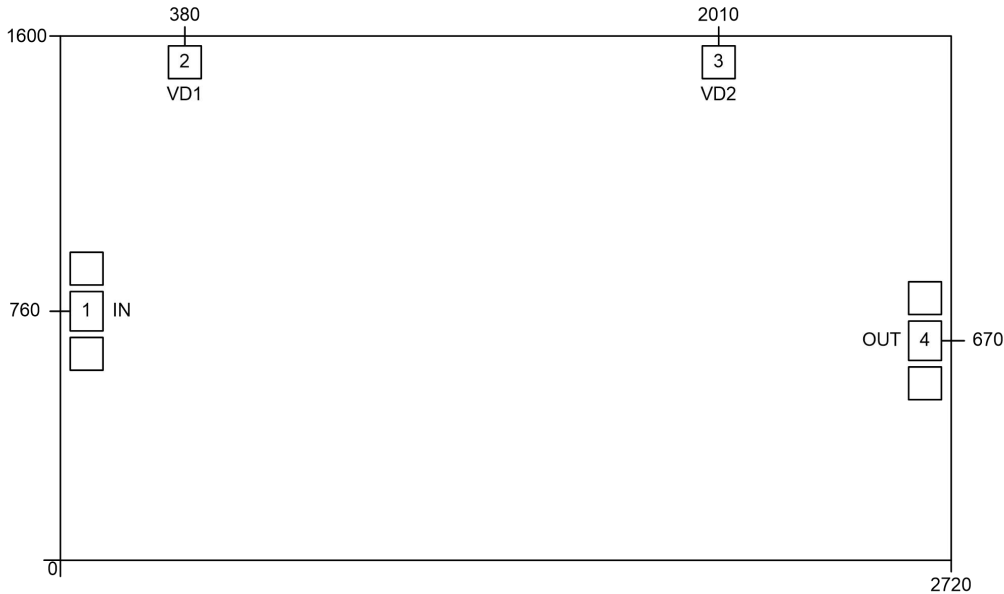


Psat vs. Frequency



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Appearance structure ²



【 2 】 All units in the figure are micrometers

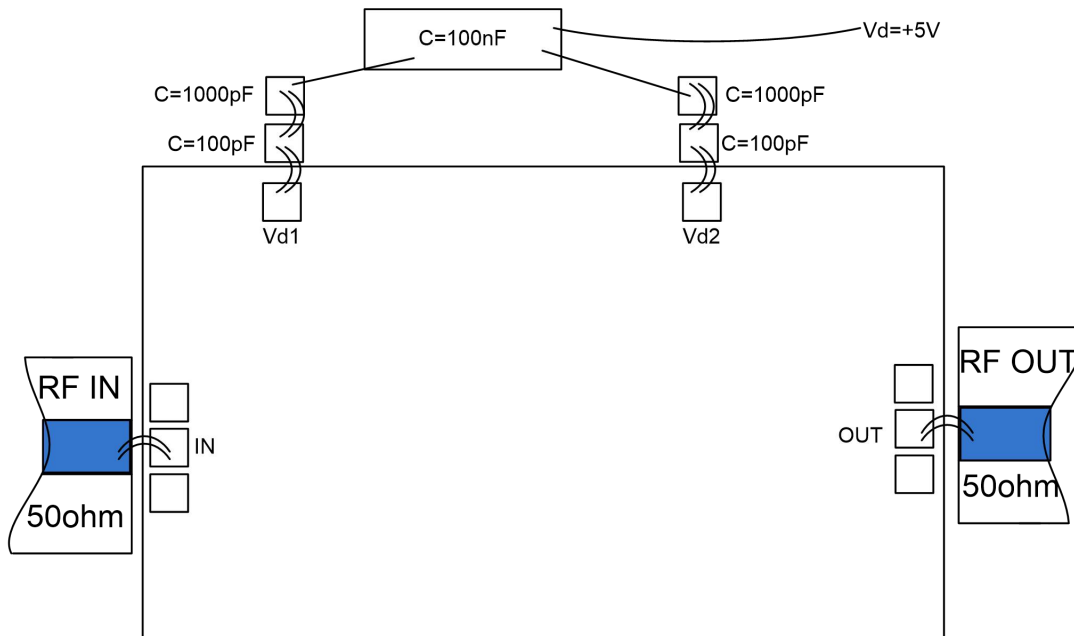
Bonding point definition

Bonding point number	Function Symbol	Functional Description
1	RFIN	RF signal input terminal, no DC blocking capacitor required
4	RFOUT	RF signal output terminal, no DC blocking capacitor required
2,3	Vd1 , Vd2	Amplifier drain bias, external 100pF , 1000pF, 100nF bypass capacitor required
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

* Ports 2 and 3 need to be powered on simultaneously.

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Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 °C and the tool (vacuum chuck) temperature reaches 265 °C . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 °C . Do not let the chip exceed 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position, the conductive glue can be vaguely seen around it . For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use $\Phi 0.025\text{mm}$ (1mil) gold wire for both ball and wedge bonding . Thermosonic bonding temperature is 150 °C . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).