GaAs MMIC Power Amplifier Chip, 6-18GHz

Performance characteristics

Frequency range: 6-18GHz
Small Signal Gain: 14 dB
P-1dB: 27.5dBm
Psat: 28.5 dBm
Power supply: +8V/380mA
50Ohm input/output
100% on-chip testing
Chip size: 1.66 x 2.43 x 0.1 mm

Product Introduction

GPA-010E is a broadband power amplifier chip based on GaAs technology, with a frequency range of 6GHz~18GHz, a small signal gain of 16.5dB, and a saturated output power of 28.5dBm. GPA-010E is powered by a single +8V power supply. The chip through-hole metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding process.

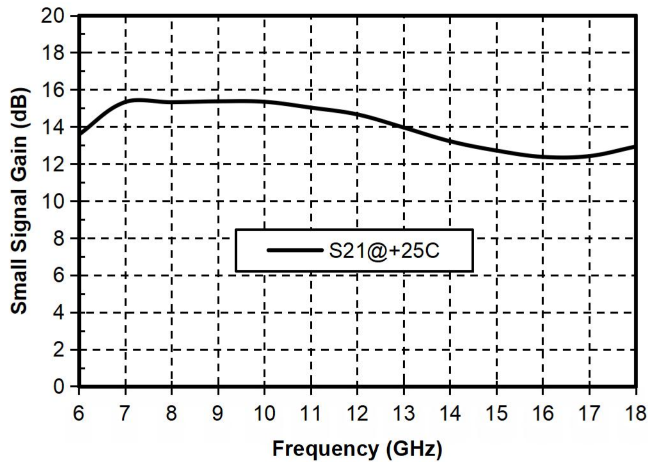
Use restriction parameter [1]	
Maximum drain voltage	+12 V
Maximum input power	+20 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

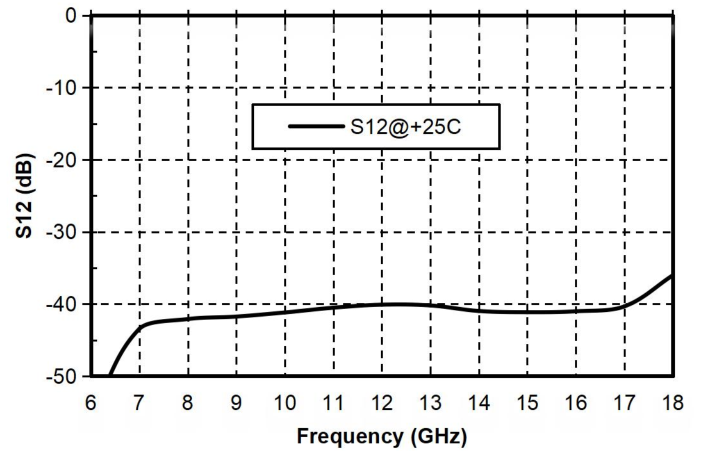
Electrical Parameters (TA = +25°C, Vd = +8 V)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range		6-18		GHz
Small Signal Gain	-	14	-	dB
Gain Flatness	-	± 1.5	-	dB
P-1dB	-	27.5	-	dBm
Psat	-	28.5	-	dBm
Input return loss	-	15	-	dB
Output return loss	-	19	-	dB
Quiescent Current		380		mA

Main index test curve

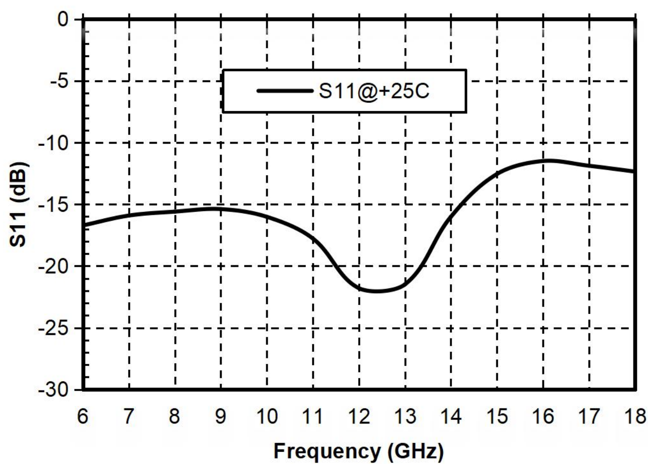
Gain vs. Frequency



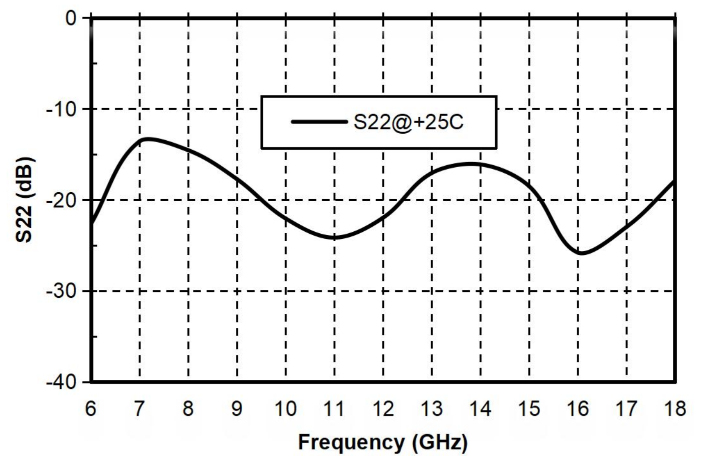
Reverse Isolation vs. Frequency



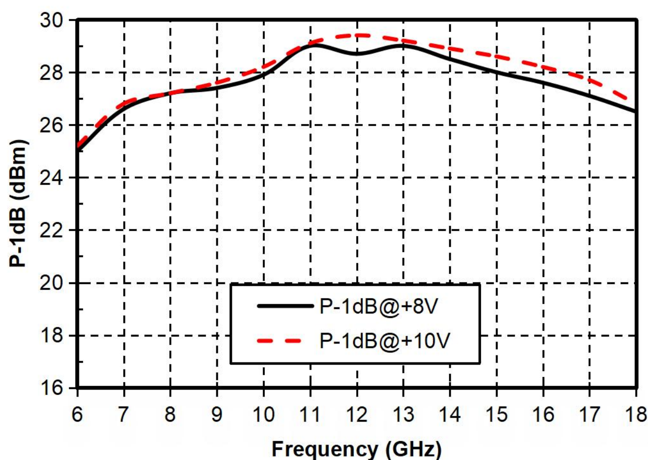
Input Return Loss vs. Frequency



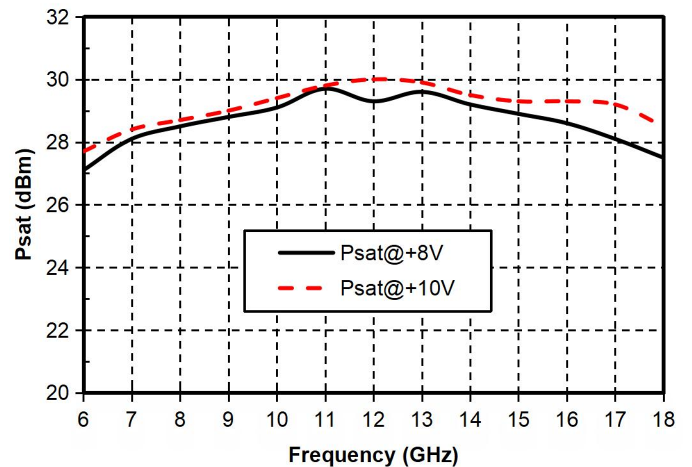
Output Return Loss vs. Frequency



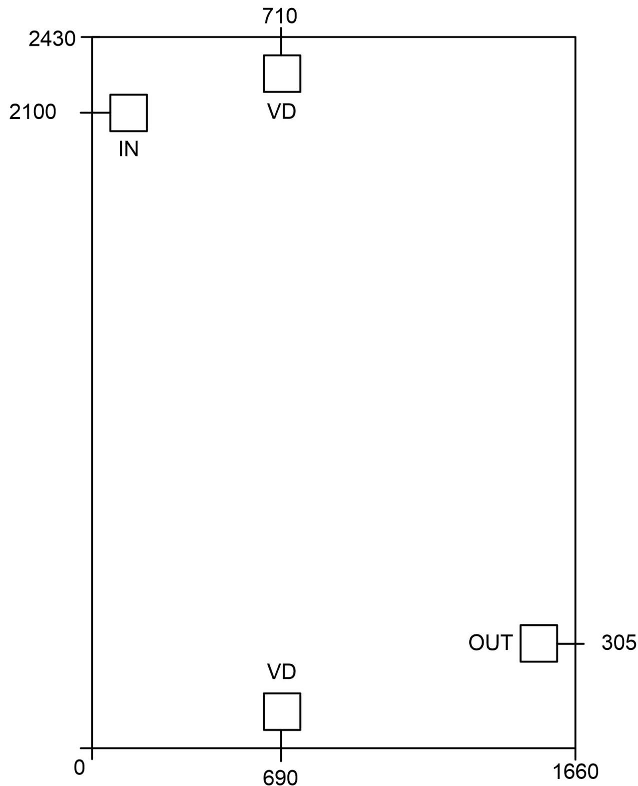
P-1 vs. Frequency



Psat vs. Frequency



Appearance structure [2]



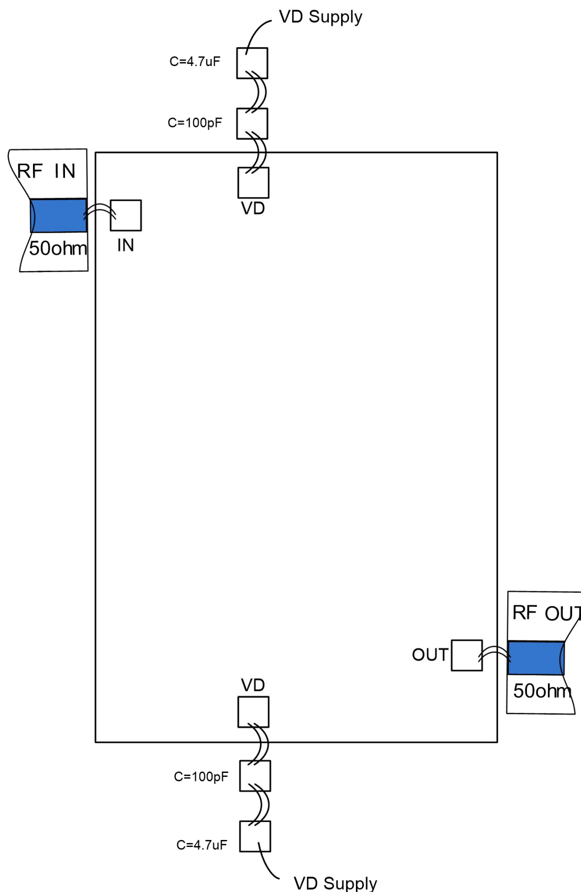
【 2 】All units in the figure are micrometers

Bonding point definition

Bonding point number	Function Symbol	Functional Description
1	RFIN	RF signal input terminal, no DC blocking capacitor required.
2	RFOUT	RF signal output terminal, no DC blocking capacitor required.
3.4*	V d	Amplifier drain bias, external 100pF , 4.7uF capacitors are required.
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC.

*Requires 3 and 4 ports to be powered on simultaneously.

Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position, the conductive glue can be vaguely seen around it . For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding .

Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).