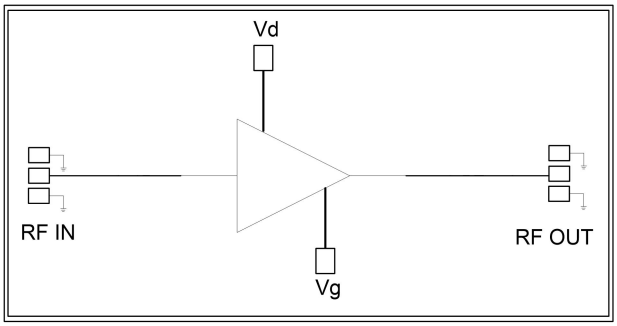
GPA-0040-22

AGC Power Amplifier Chip, DC-40GHz

Performance characteristics

Frequency range: DC-40GHz
Small signal gain: 12dB
Noise figure: 5dB
Psat: 22dBm
Power supply: + 7V / 160mA
50Ohm input / output
100% on-chip testing
Chip size: 2.5 x 1.2 x 0.1mm

Functional Block Diagram



Product Introduction

GPA-0040-22 is an ultra-wideband distributed amplifier chip based on pHEMT technology, with a frequency range covering DC~40GHz , a small signal gain of 12dB , and a saturated output power of 22dBm. IPA-0040-22 can achieve automatic gain control by tuning the VC control terminal voltage. The chip through-hole metallization process ensures good grounding, and the back side is metallized, which is suitable for eutectic sintering or conductive adhesive bonding process.

Use restriction parameter 1	
Maximum drain voltage	+9V
Maximum gate bias	-2V
Maximum input power	+18dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

Electrical Parameters (T_A = +25°C, Vd = +7 V)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range		DC-40		GHz
Small Signal Gain		12		dB
Noise Figure		5		dB
P-1dB*(negative pressure condition)		20		dBm
Psat*(negative pressure condition)		22		dBm
Input return loss		15		dB
Output return loss		15		dB
Quiescent Current		160		mA
* By tuning the Vg terminal voltage from -2V to 0V , 160mA is achieved , and the Vg terminal voltage is expected to be -0.25V ; the Vg terminal can be left floating, and the current is 185mA when it is left floating.				

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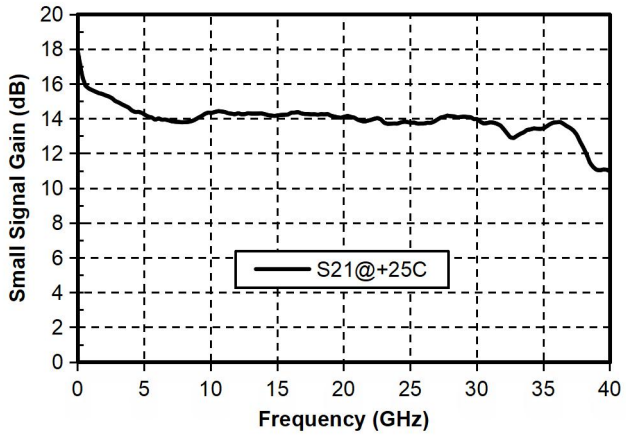
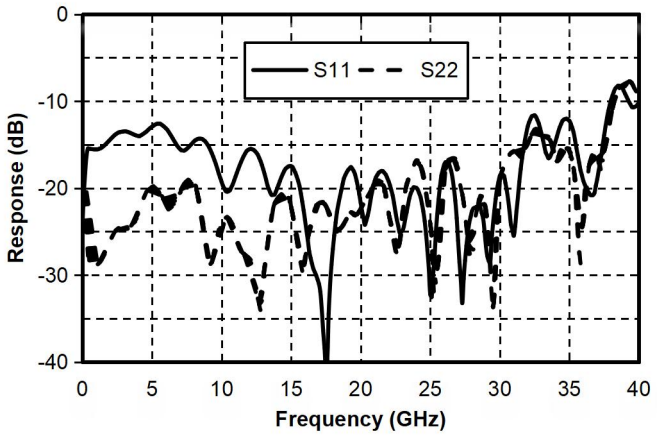
Main indicator test curve @+ 7 V, 160 mA

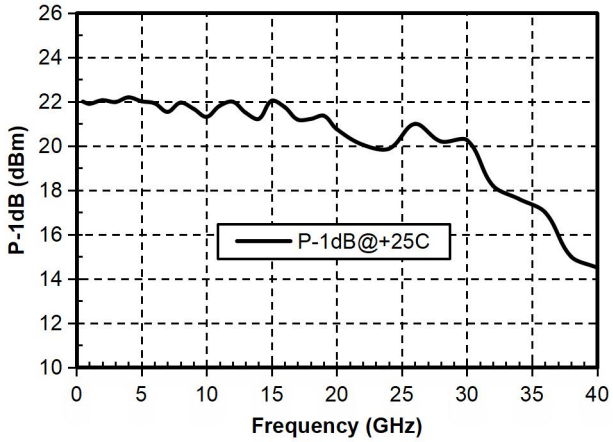
Gain vs. Frequency



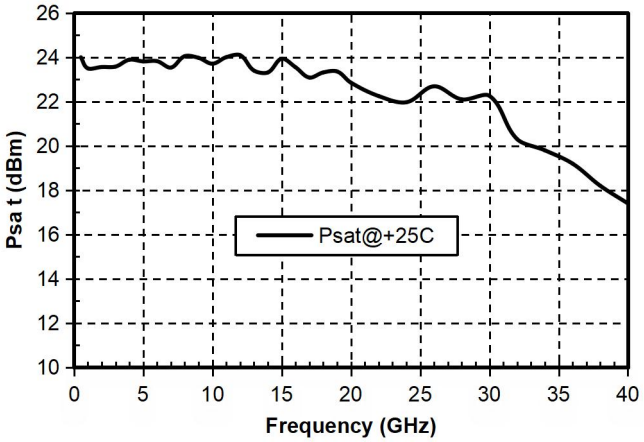
Input/output return loss



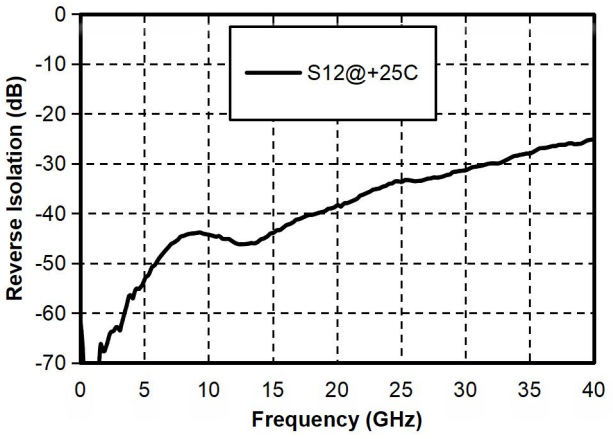
P-1dB vs. Frequency



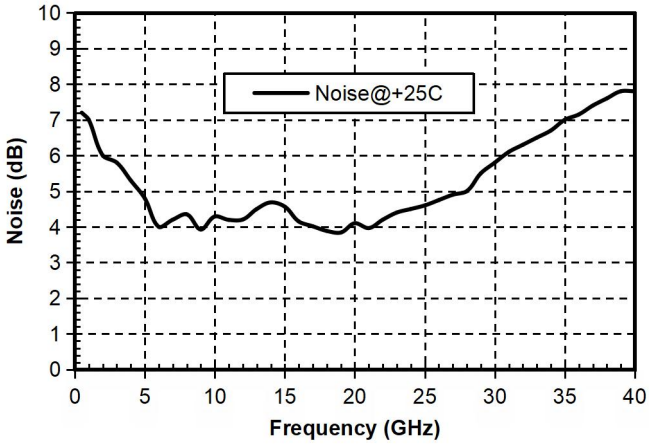
Psat vs. Frequency



Reverse Isolation vs. Frequency



Noise Figure vs. Frequency



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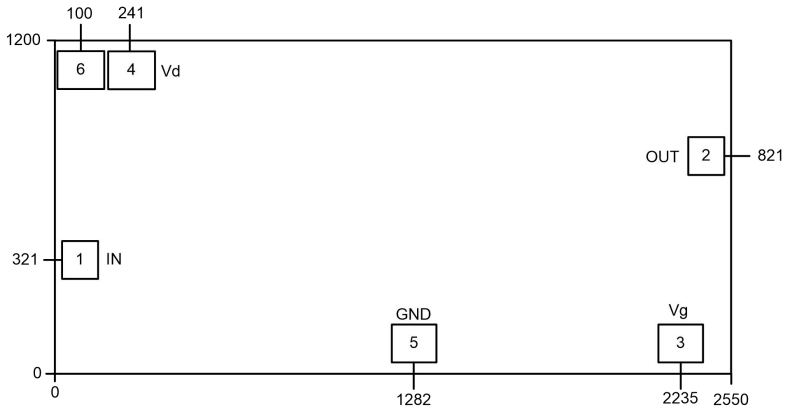
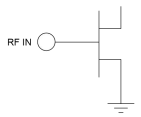
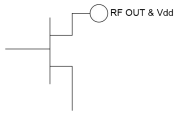
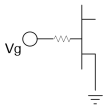
Appearance structure 2



【2】All units in the figure are micrometers

Bonding point definition			
Bonding point number	Function Symbol	Functional Description	Equivalent Circuit
1	RFIN	RF signal input terminal, DC blocking capacitor needs to be added	
2	RFOUT	At the RF signal output end, a DC blocking capacitor needs to be added	
3	Vg	Amplifier gate bias, requires external 100pF bypass capacitor	
4	V d	Amplifier drain bias, requires external 100pF bypass capacitor	
5	GND	Ground pressure point for probe testing	
6	Vctl	Amplifier gain control terminal, requires external 100pF bypass capacitor	
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC	

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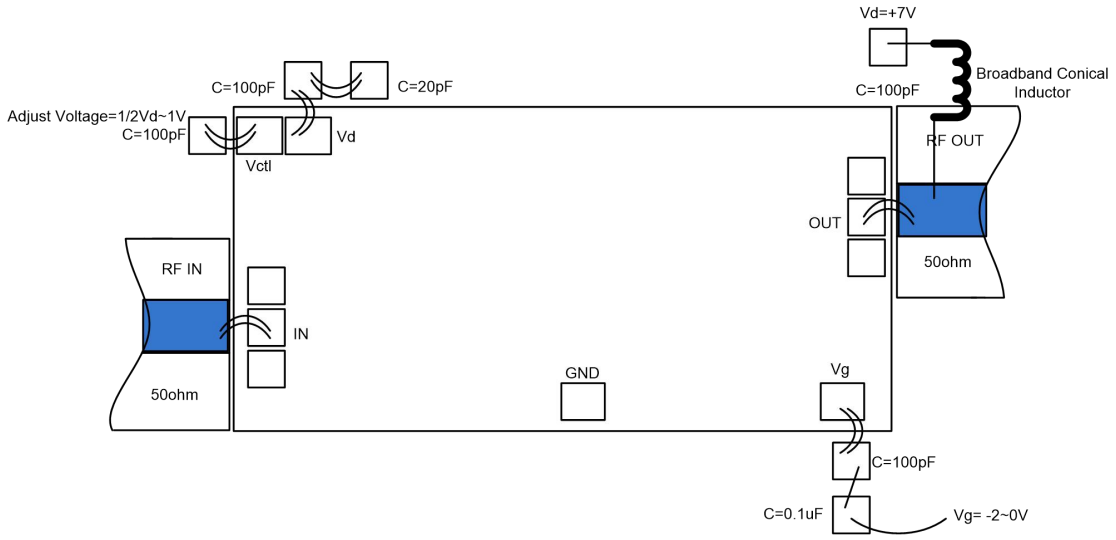
Recommended assembly drawing



Note

1. VD terminal to ground .
2. The power supply is located at the chip RF output port and is powered by a broadband conical inductor .
3. The gain control terminal (Vctl) adjusts the voltage from 1/2 chip power supply voltage to +1V , which can achieve chip (1V) 0dB ~ (3.5V) 12dB gain output tuning.
4. +6V power supply chip can also work. When working at +6V , the output gain increases by 2~3dB and the output power decreases by 2~3dB .

Notice

- The chip needs to be stored in an anti-static container and kept in a nitrogen environment.
- Do not attempt to clean the bare die surface using wet chemical methods.
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: Bare chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive bonding. The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold-tin ratio of 80/20 . The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃. When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃. Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive glue dispensed should be as small as possible. After the chip is placed in the installation position , the conductive glue should be vaguely visible around it . For curing conditions, please follow the information provided by the conductive glue manufacturer.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding.

Thermo-ultrasonic bonding temperature is 150 ° C. The pressure of the wedge for ball bonding is 40~50gf , and the pressure of the wedge bonding is 18~22gf . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate) .