GPA-0015B

GaAs MMIC Power Amplifier Chip, DC-15GHz

Performance characteristics

Frequency range: DC-15 GHz
Small Signal Gain: 18 dB
P-1dB: 25.5 dBm
Psat: 26.5 dBm
Power supply: +8V@270mA
50Ohm input/output
100% on-chip testing
Chip size: 3.12 x 1.62 x 0.1mm

Product Introduction

GPA-0015B is a broadband amplifier chip based on GaAs technology, with a frequency range of DC-15GHz, a small signal gain of 18dB, and a Psat output power of 26.5dBm.The chip via metallization process ensures good grounding, and the back side is metallized for eutectic sintering process.

Use restriction parameter [1]	
Maximum drain voltage	+12 V
Maximum input power	+20 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd = +8 V , Ids= 270 mA)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency range		DC-15		GHz
Small signal gain	-	18	-	dB
Gain flatness		± 1.6		dB
P-1dB	-	25.5	-	dBm
Psat	-	26.5	-	dBm
Input return loss	-	19	-	dB
Output return loss	-	21	-	dB
*By tuning the Vg terminal voltage from -2V to 0V, the recommended Vg terminal voltage is -0.65V .				

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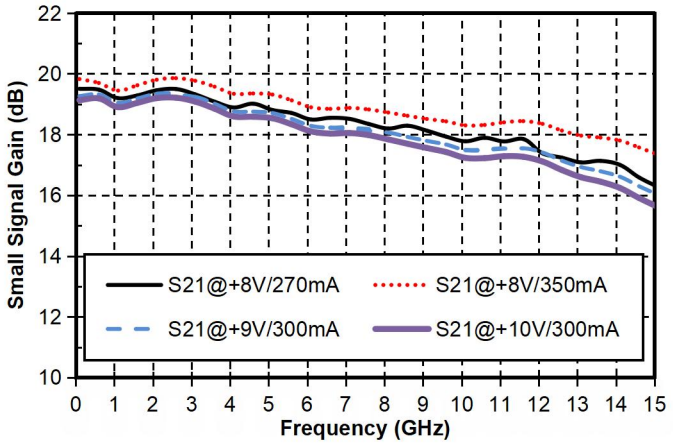
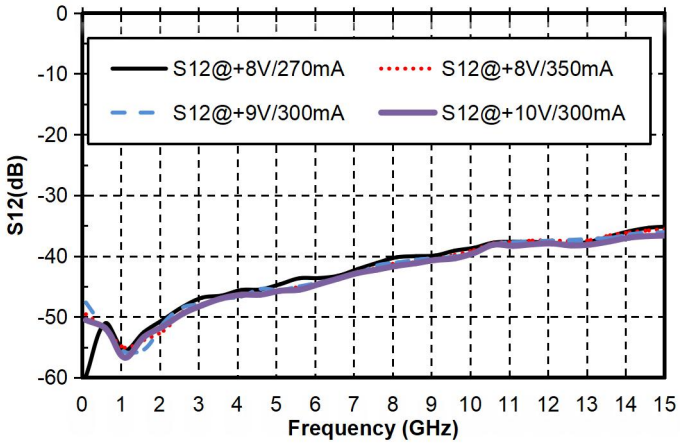
Main index test curve

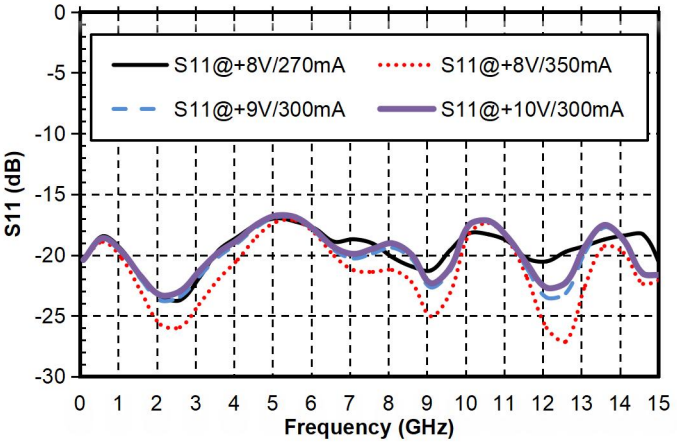
Gain vs. Frequency



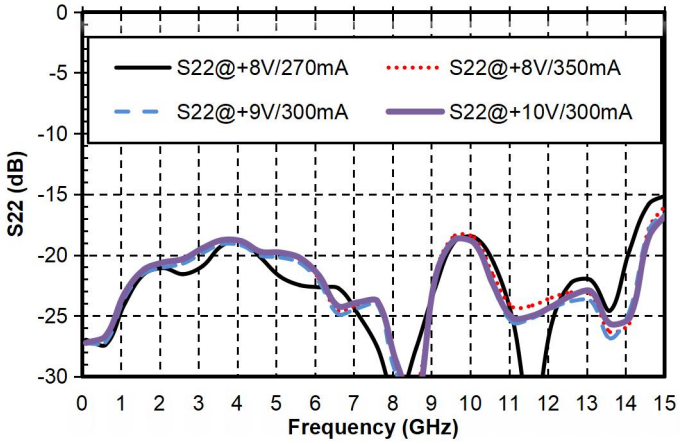
Reverse Isolation vs. Frequency



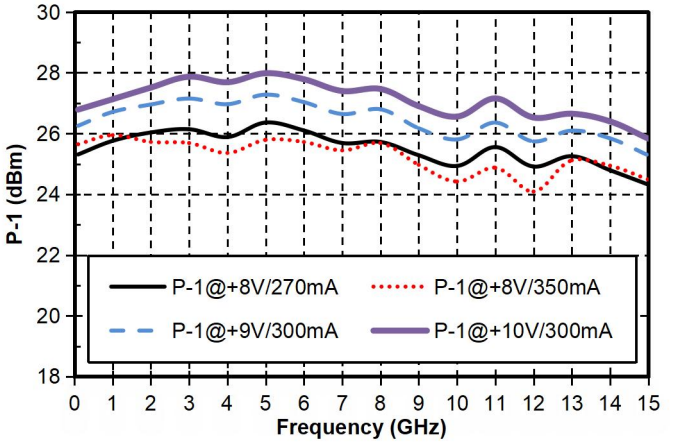
Input Return Loss vs. Frequency



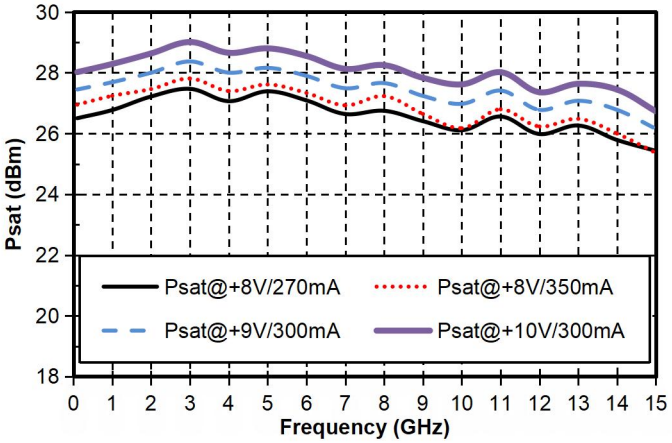
Output Return Loss vs. Frequency



P -1 vs. Frequency



P sat vs. frequency



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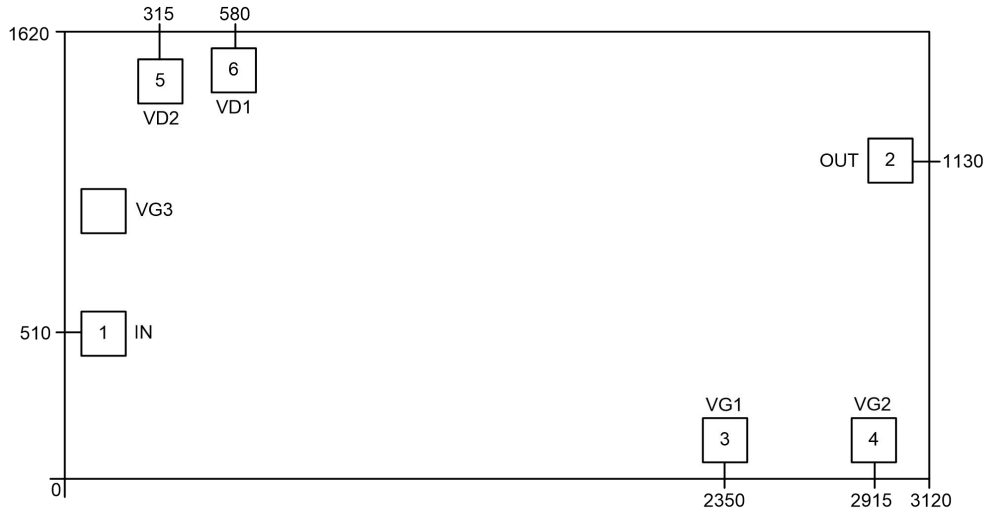
Appearance structure [2]



【 2 】The units in the figure are all micrometers (dimensional tolerance: ±100um.)

Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and no DC blocking capacitor is required
2	RF OUT 、VD	The signal output terminal is connected to a 50 ohm circuit, and a DC blocking capacitor needs to be added. An external DC bias network is connected to provide drain current. Please refer to the following application circuit or contact the manufacturer*
3	VG1	Amplifier gate bias , external 100pF , 0.01uF bypass capacitor required
4	VG2	Amplifier gate bias , external 100pF , 4.7uF bypass capacitors are required
5	VD2	An external 100pF bypass capacitor is required to ground
6	VD1	An external 4.7u F bypass capacitor is required and connected to ground
Chip bottom	GND	needs to be in good contact with the RF and DC grounds

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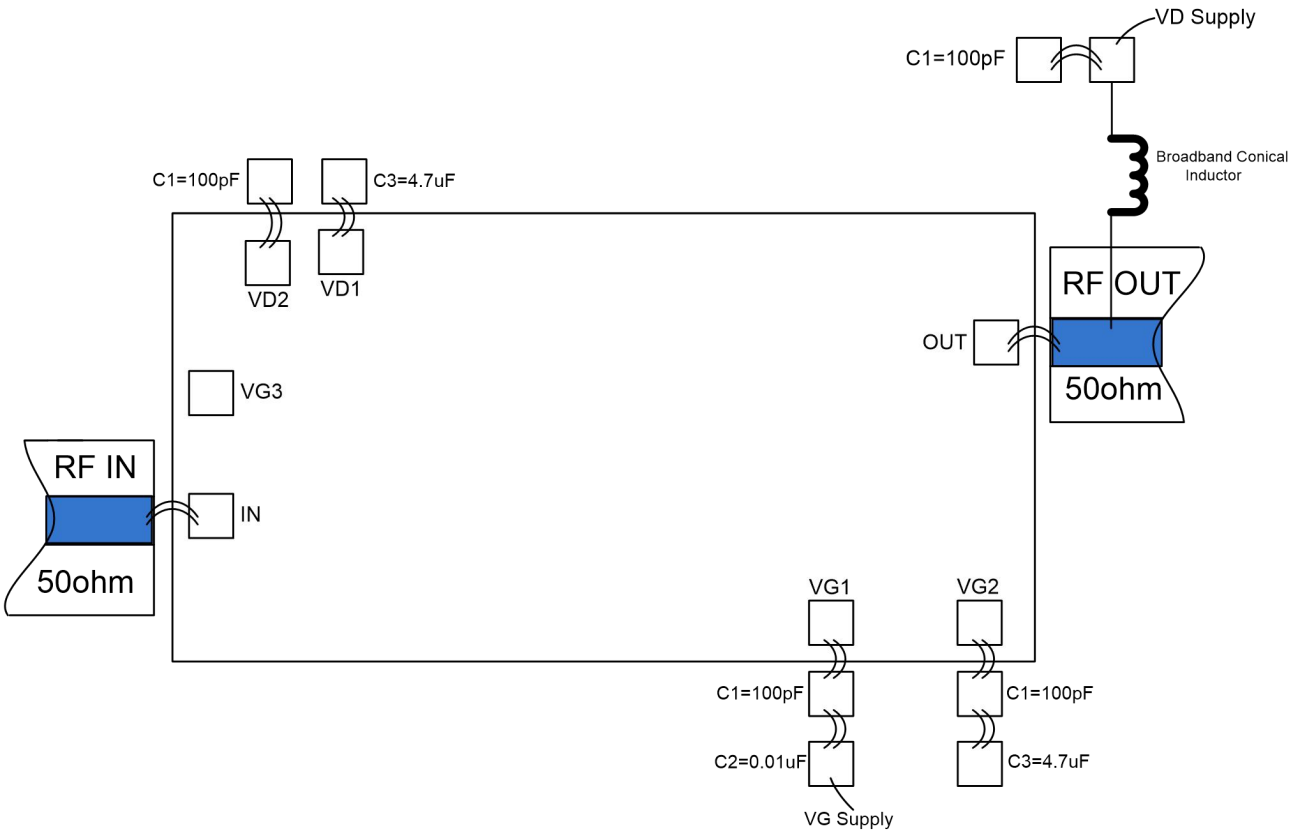
Recommended assembly diagram



Notice

- The chip must be stored in an anti-static container and kept in a nitrogen environment.
- bare die surface using wet chemical methods .
- Please strictly follow the ESD protection requirements to avoid static damage to the bare chip.
- General operation: Please use precision pointed tweezers to pick up bare chips. Avoid touching the chip surface with tools or fingers during operation.
- Rack mounting operation suggestions: AuSn solder eutectic sintering process can be used for bare chip mounting . The mounting surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold -tin ratio of 80/20 . The working surface temperature reaches 255 ℃ and the tool (vacuum chuck) temperature reaches 265 ℃ . When the high-temperature mixed gas (nitrogen-hydrogen ratio of 90/10) is blown to the chip, the temperature at the top of the tool should be raised to 290 ℃ . Do not let the chip exceed 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding operation suggestions: Use Φ0.025mm (1mil) gold wire for both ball and wedge bonding . Thermosonic bonding temperature is 150 ℃ . The pressure of the wedge bonding knife is 40~50gf for ball bonding and 18~22gf for wedge bonding . Use the smallest possible ultrasonic energy. The bonding starts at the pressure point on the chip and ends at the package (or substrate).