

### GaAs MMIC Power Amplifier Chip, DC- 13 GHz

#### Performance characteristics

Frequency range: DC - 13 GHz

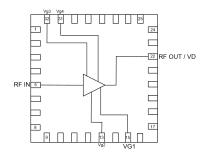
Small signal gain: 18dB Gain flatness: ± 2.5dB

P-1dB: 25 dBm Psat : 2 6 dBm

Power supply: +8V / 300mA

50Ohm input / output Chip size: QFN 5X5

### **Functional Block Diagram**



### **Product Introduction**

GPA- 0013B-CQ5 is an ultra-wideband distributed amplifier chip based on pHEMT technology, with a frequency range of DC~ 13 GHz, a small signal gain of 18 dB, and a saturated output power of 26 dBm. This chip uses a 5 x 5 mm ceramic surface mount package to achieve airtight packaging. The surface of the pin pad is gold-plated and is suitable for reflow soldering installation.

Use restriction parameter <sup>1</sup>		
Maximum drain voltage	+1 0 V	
Maximum gate bias	-3V	
Maximum input power	+20dBm	
Operating temperature	-55 ~ +85°C	
Storage temperature	-65 ~ +150°C	

[1] Exceeding any of these maximum limits may cause permanent damage.

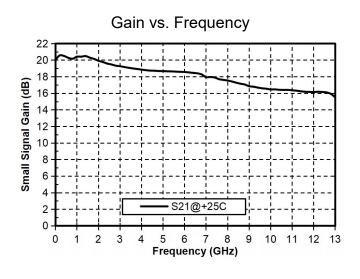
Electrical parameters (Ta=+25°C, Vd = + 8V, Ids= 300 mA)					
Index	Minimum	Typical Value	Maximum	Unit	
Frequency Range	DC-1 3		GHz		
Small Signal Gain	-	18	-	dB	
Gain Flatness	-	± 2.5	-	dB	
P-1dB	-	25	-	dBm	
Psat	-	26	-	dBm	
Input return loss	-	20	-	dB	
Output return loss	-	20	-	dB	

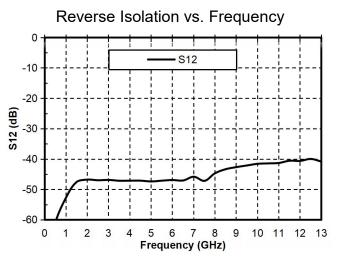
<sup>\*</sup>By tuning the Vg 1 terminal voltage from -2V to 0V, 300 mA is achieved and the Vg terminal voltage is expected to be -0.6 V.

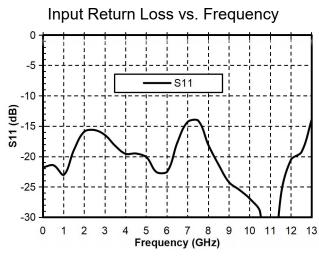


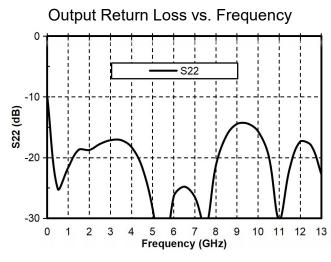
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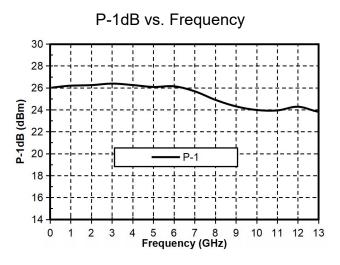
### Main index test curve

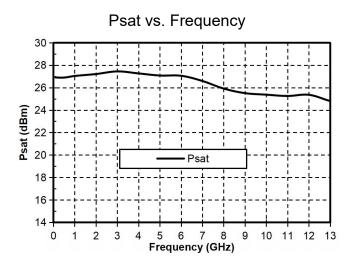








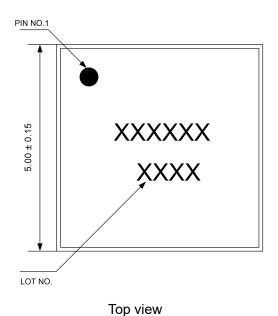


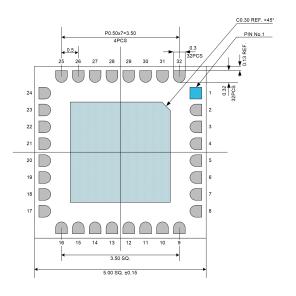




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### Appearance structure





Bottom view

5.00 ± 0.15

Side View

The units in the figures are all in millimeters , and the tolerance is  $\pm 0.15$  mm.

Pin Definition				
Bonding point number	Function Symbol	Functional Description		
5	RFIN	The signal input terminal is connected to a 50 ohm circuit, and a DC blocking capacitor needs to be added		
22	RFOUT	The signal output terminal is connected to a 50 ohm circuit, and a DC blocking capacitor needs to be added .  An external DC bias network is connected to provide drain current.		
15	Vg 1	Amplifier gate bias, requires external bypass capacitor		
13, 31, 32		Ground , external bypass capacitor required		
4, 6, 21, 23	GND	The pins need to be well grounded to the RF and DC grounds		

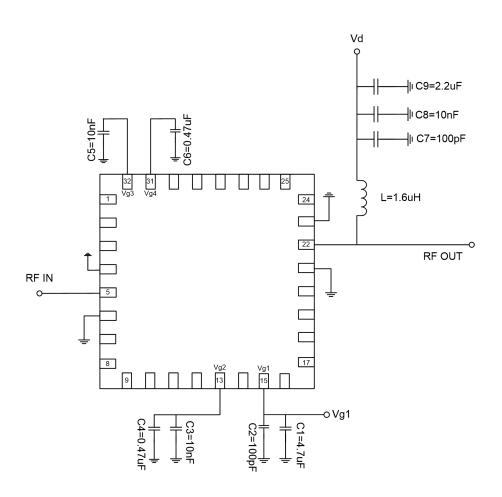


# **GP A- 0013B-CQ5**

Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC
Other	NC	Floating pin, can be grounded

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### Recommended Circuit



### Precautions for use

- Sealing material: Ceramic material that meets ROSH standards
- Lead frame material: copper alloy
- Lead surface plating: gold, gold layer thickness greater than 0.3um MIN
- Maximum reflow peak temperature: 260 ℃