

GaAs MMIC Power Amplifier Chip, DC-12GHz

Performance characteristics

Frequency range: DC-12GHz

Small Signal Gain: 14 dB

P-1dB: 30.5 dBm

Psat: 31.5 dBm

Power supply: +12V@350mA

50Ohm input/output

100% on-chip testing

Chip size: 2.04 x 1.78 x 0.1mm

Product Introduction

GPA -0012B is a broadband amplifier chip based on GaAs technology, with a frequency range of DC-12GHz, a small signal gain of 14dB, and a Psat output power of 31.5dBm . The chip via metallization process ensures good grounding, and the back side is metallized for eutectic sintering process.

Use restriction parameter ¹

Maximum drain voltage	+15 V
Maximum input power	+25 dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical parameters (Ta=+25°C, Vd = +12 V , Ids= 350 mA)

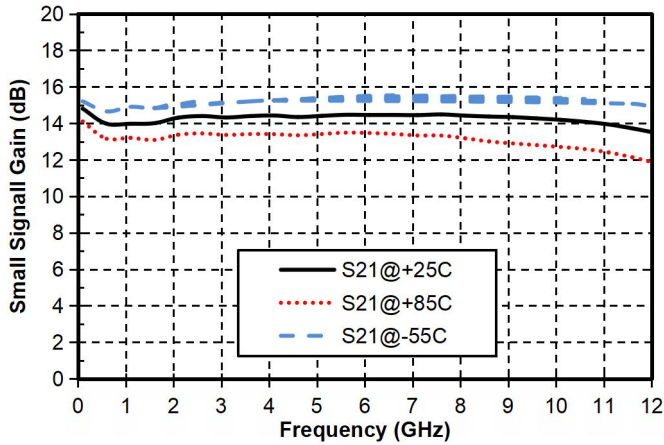
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	DC-12			GHz
Small Signal Gain	-	14	-	dB
Gain Flatness	± 0.7			dB
P-1dB	-	30.5	-	dBm
Psat	-	31.5	-	dBm
Noise Figure	-	3.5	-	dB
OIP3 with 20dBm output	-	40	-	dBm
IMD3 with 20dBm output	-	-40	-	dBc
Input return loss	-	16	-	dB
Output return loss	-	21	-	dB

*By tuning the Vg terminal voltage from -2V to 0V, the recommended Vg terminal voltage is -0.85V .

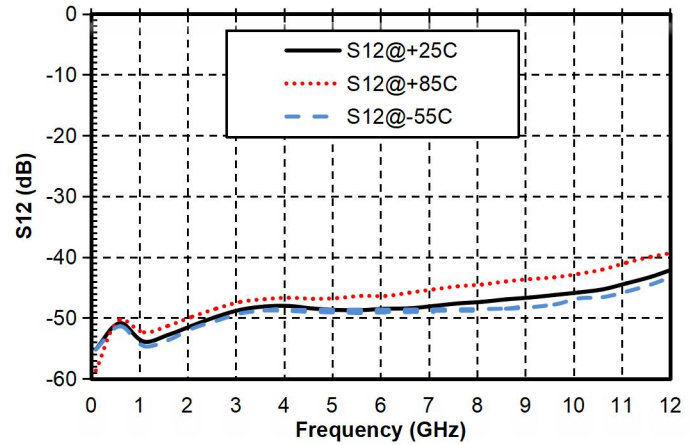
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Main index test curve

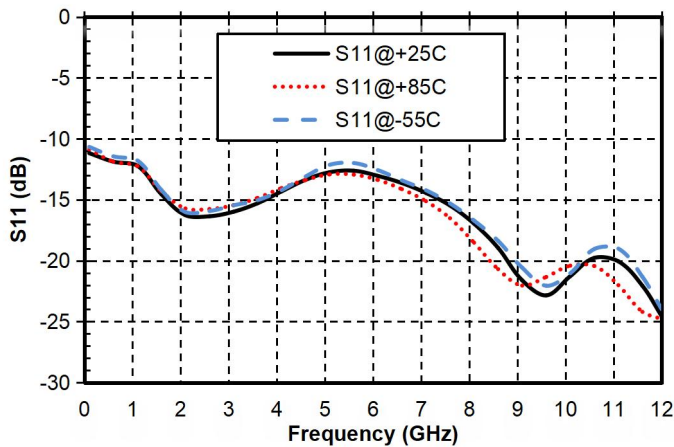
Gain vs. Frequency



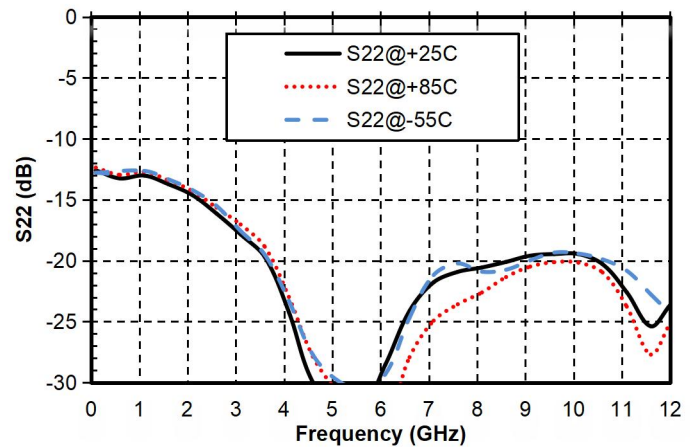
Reverse Isolation vs. Frequency



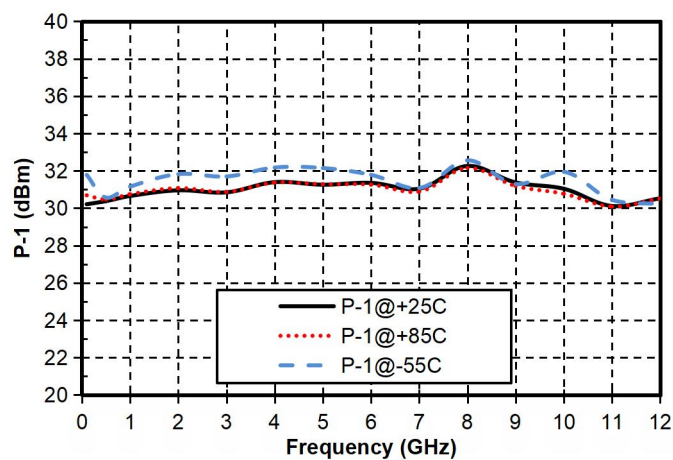
Input Return Loss vs. Frequency



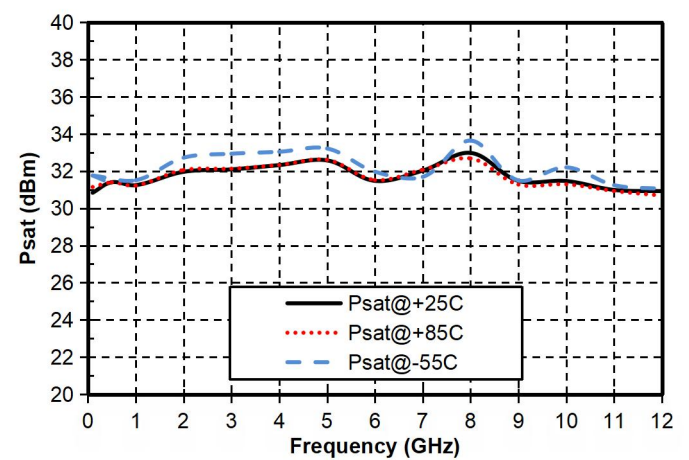
Output Return Loss vs. Frequency



P-1 vs. Frequency



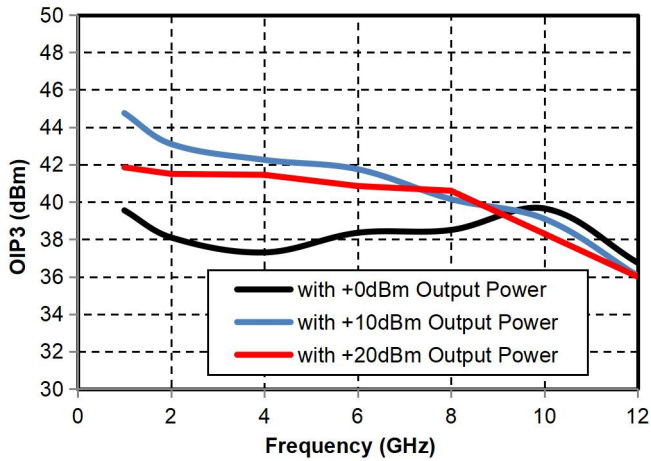
P sat vs. frequency



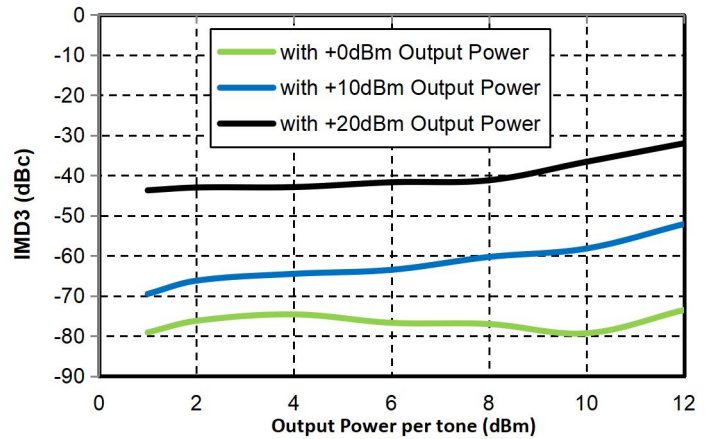
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Main index test curve

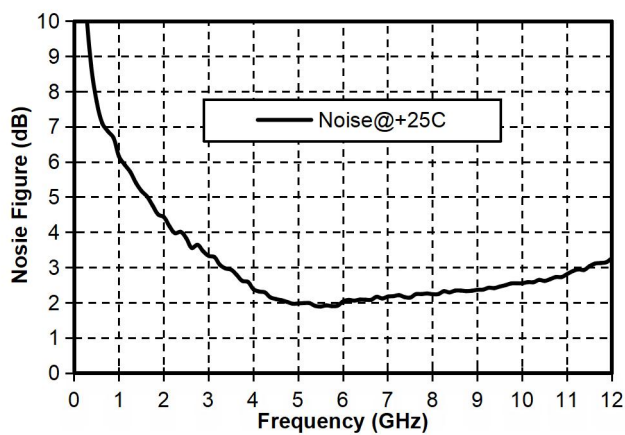
OIP3 vs. Frequency



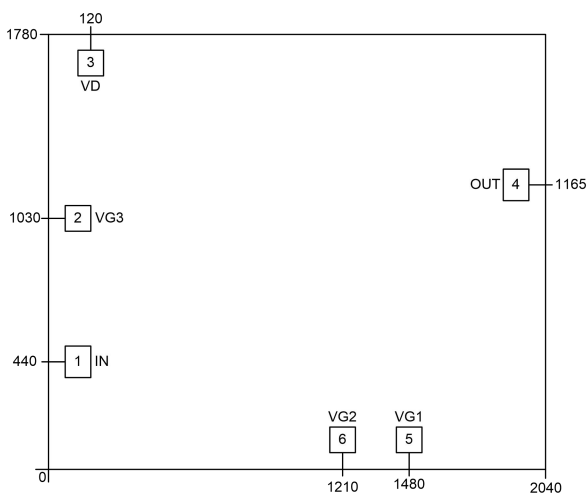
IMD3 vs. Frequency



Noise Figure vs. Frequency



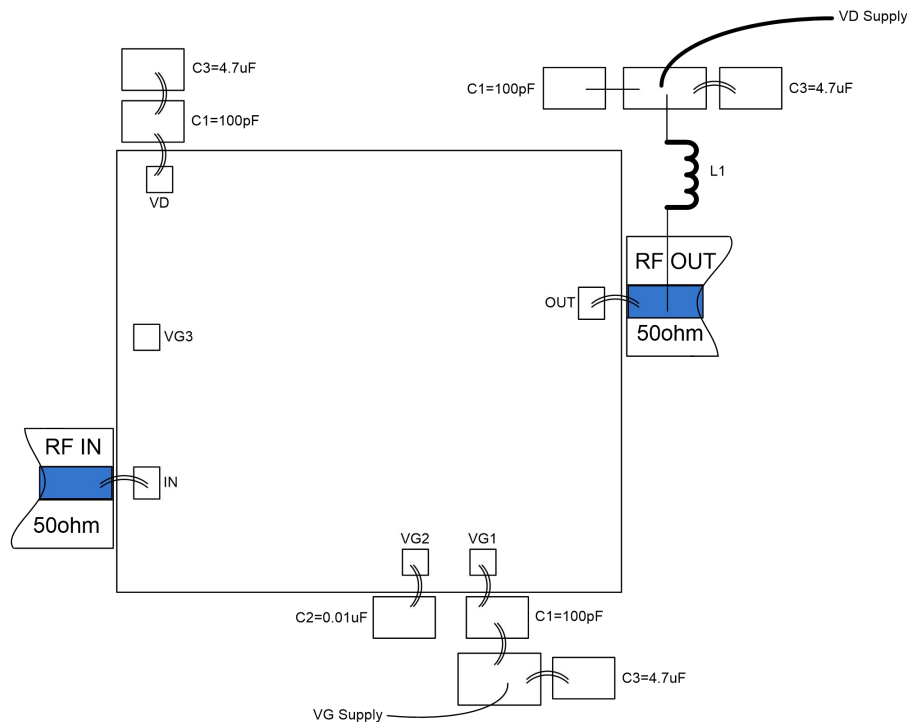
Appearance structure ²



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Bonding point definition		
Bonding point number	Function Symbol	Functional Description
1	RF IN	The signal input terminal is connected to a 50 ohm circuit, and a DC blocking capacitor needs to be added
4	RF OUT , VD	The signal output terminal is connected to a 50 ohm circuit, and a DC blocking capacitor needs to be added. An external DC bias network is connected to provide drain current. Please refer to the following application circuit or contact the manufacturer*
5	VG1	Amplifier gate bias , external 100pF , 4.7uF bypass capacitors are required
6	VG2	Amplifier gate bias , external 0.01uF bypass capacitor is required to ground
3	VD	Need to connect external 100pF , 4.7uF bypass capacitor to ground
Chip bottom	GND	needs to be in good contact with the RF and DC grounds

Recommended assembly diagram



【 2 】 The units in the figure are all micrometers , and the dimensional tolerance is $\pm 50\mu\text{m}$.