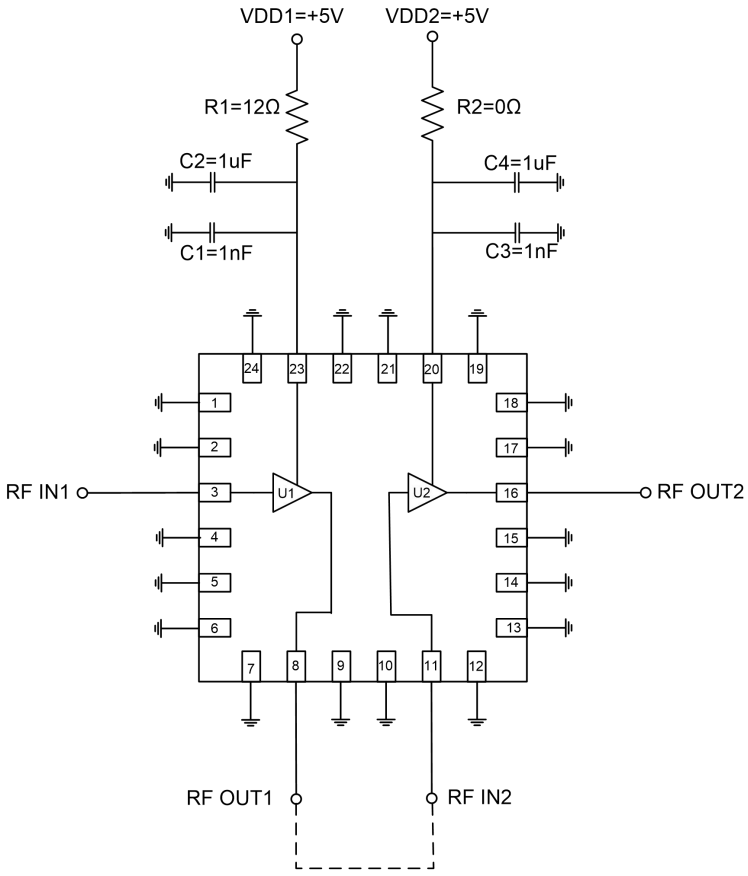
GLA-012017C-CQ4

GaAs MMIC High Linearity, Low Noise Amplifier Chip, 1.2 - 1.7 GHz

Product Introduction

GLA-012017C-CQ4 is a high linearity, low noise amplifier chip with a frequency range of 1.2GHz~1.7GHz.
The amplifier shares three operating modes.
Working mode 1 is RFIN1 input and RFOUT1 output;
Working mode 2 is RFIN2 input and RFOUT2 output;
Working mode three is RFIN1 input, RFOUT1 and RFIN2 are interconnected, and RFOUT2 is output.
The chip adopts 4 x 4 mm ceramic surface mount package, and the surface of the pin pad is gold-plated, which is suitable for reflow soldering installation process.

Recommended Circuit



Use restriction parameter [1]

Maximum drain voltage	+7V
Maximum input power	+20dBm
Operating temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】Exceeding any of these maximum limits may cause permanent damage.

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Working mode 1

Performance characteristics

- Frequency range: 1.2 - 1.7 GHz
- Small Signal Gain: 21 dB
- Gain flatness : ± 0.3 dB
- Noise figure : 0.6 dB
- P-1dB: 19.5 dBm
- OIP3 : 34 dBm

Electrical performance parameters (TA = +25°C, Vd = +5V, 50Ω system)

Index	Test Conditions	Minimum	Typical Value	Maximum	Unit
Frequency Range		-	1.2-1.7	-	GHz
Small Signal Gain		-	21	-	dB
Gain Flatness		-	±0.3	-	dB
Input return loss		-	11	-	dB
Output return loss		-	24	-	dB
Reverse Isolation		-	31	-	dB
P-1		-	19.5	-	dBm
OIP3	Pout = 0 dBm/tone, Δf = 1 MHz	-	34	-	dBm
Noise Figure		-	0.6	-	dB
Quiescent Current		-	75	-	mA

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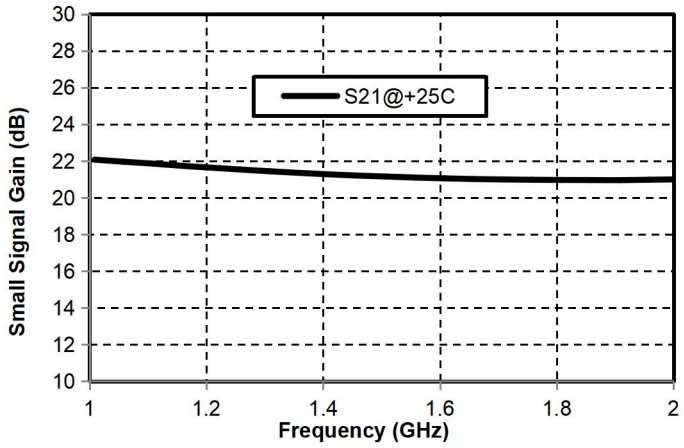
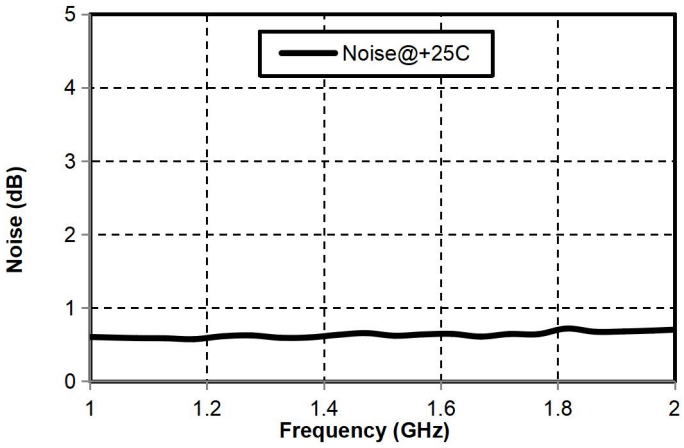
GaAs MMIC Low Noise Amplifier Chip, 1.2-1.7 GHz

Main index test curve

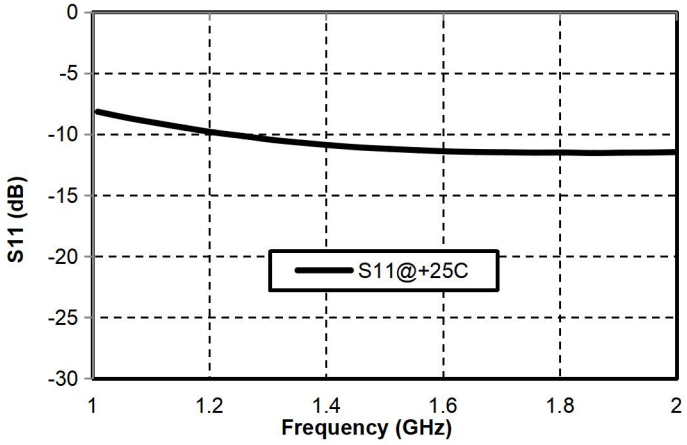
Small Signal Gain vs. Frequency



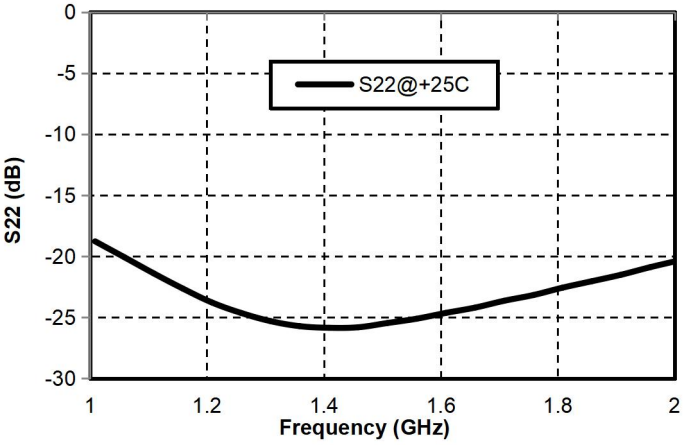
Noise Figure vs. Frequency



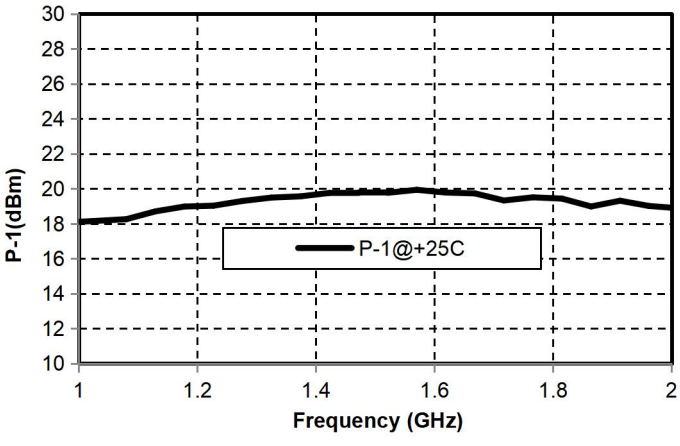
Input Return Loss vs. Frequency



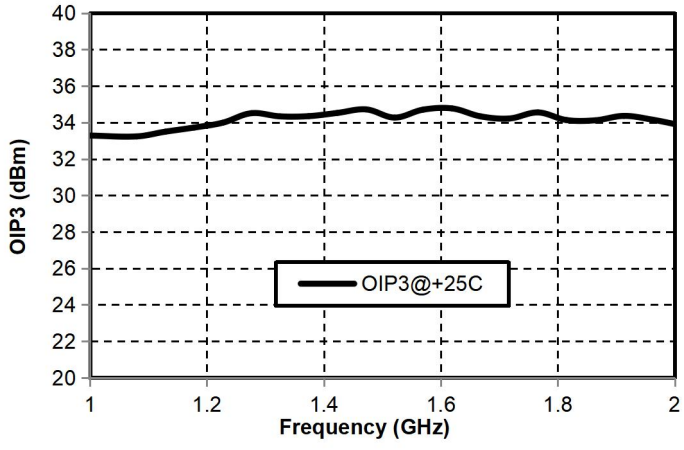
Output Return Loss vs. Frequency



P-1dB vs. Frequency



OIP3 vs. Frequency



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GaAs MMIC Low Noise Amplifier Chip, 1.2-1.7 GHz

Working mode 2

Electrical performance parameters (TA = +25°C, Vd = +5V, 50Ω system)					
Index	Test Conditions	Minimum	Typical Value	Maximum	Unit
Frequency Range		-	1.2-1.7	-	GHz
Small Signal Gain		-	17	-	dB
Gain Flatness		-	± 0.4	-	dB
Input return loss		-	12	-	dB
Output return loss		-	11	-	dB
Reverse Isolation		-	21	-	dB
P-1		-	20.5	-	dBm
OIP3	Pout = 0 dBm/tone, Δf = 1 MHz	-	35.5	-	dBm
Noise Figure		-	1.4	-	dB
Quiescent Current		-	75	-	mA

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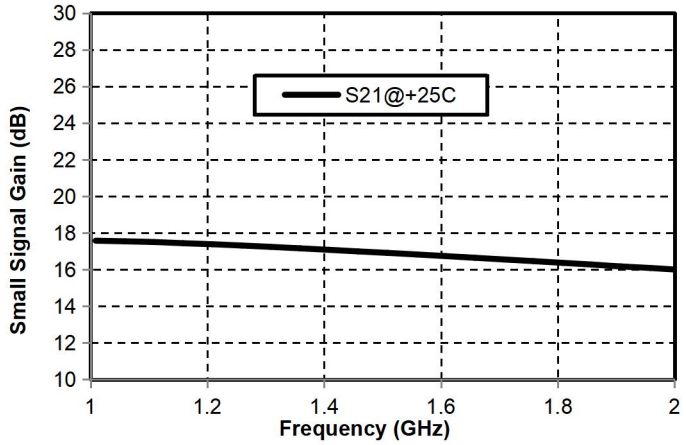
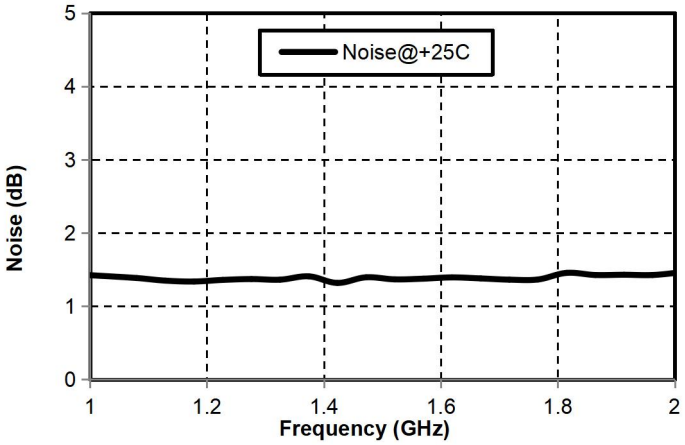
To test the curve

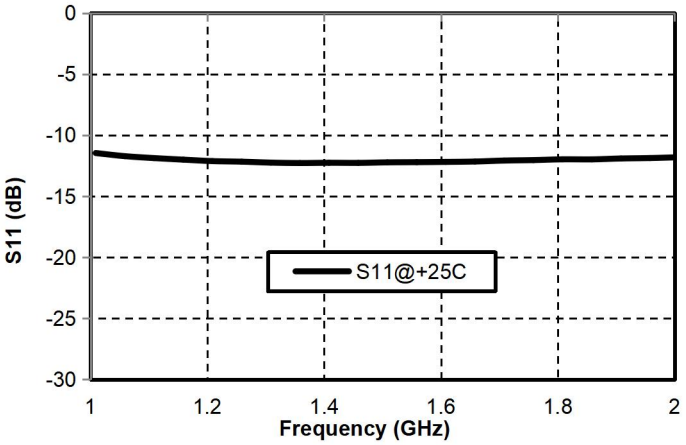
Small Signal Gain vs. Frequency



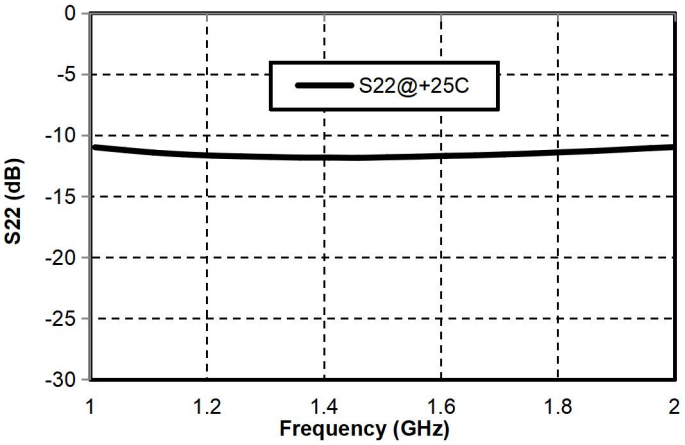
Noise Figure vs. Frequency



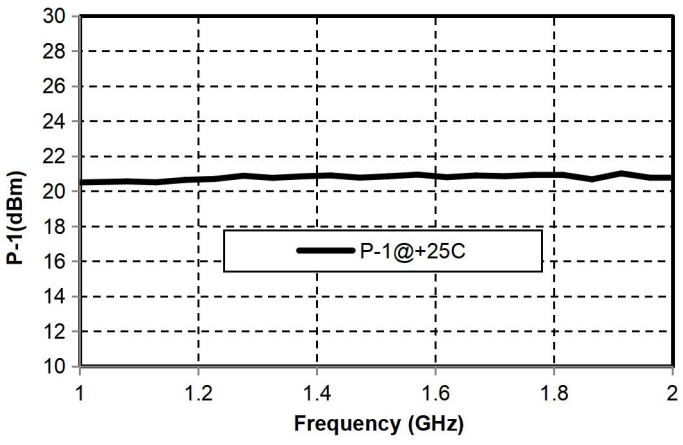
Input Return Loss vs. Frequency



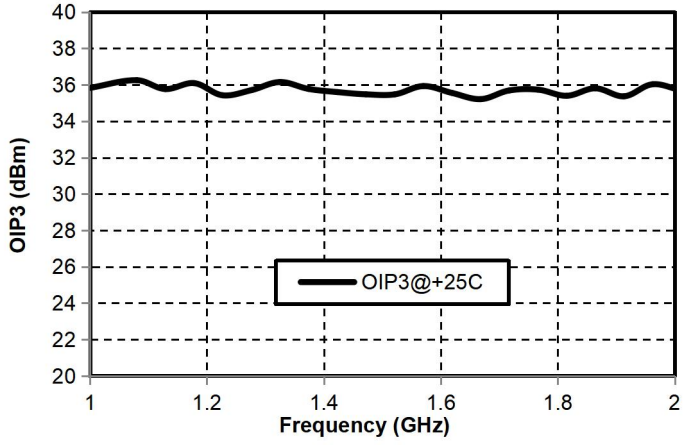
Output Return Loss vs. Frequency



P-1dB vs. Frequency



OIP3 vs. Frequency



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Standard Circuit

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Performance characteristics	
● Frequency range: 1.2 - 1.7 GHz ● Small Signal Gain: 38 dB ● Noise figure: 0.6dB typ. ● P -1 dB: 20.5dBm ● Power supply: + 5V /150mA ● 50Ohm input / output ● 100% on-wafer testing ● Chip size: QFN 4X4	

Electrical performance parameters (TA = +25°C, Vd = +5V)

Index	Minimum	Typical Value	Maximum	Unit
Frequency Range		1.2-1.7		G Hz
Small Signal Gain	-	38	-	dB
Gain Flatness	-	± 1.2	-	dB
Noise Figure	-	0.6	-	dB
P -1 dB	-	20.5	-	dBm
Psat	-	21	-	dBm
OIP3 (Pout=0dBm/tone , Δf =1MHz)		36		dBm
Input return loss	-	10	-	dB
Output return loss	-	10	-	dB
Reverse Isolation	-	52	-	dB
Quiescent Current	-	150	-	mA

* The test results are for the connection between RFOUT1 and RFIN2 outside the chip .

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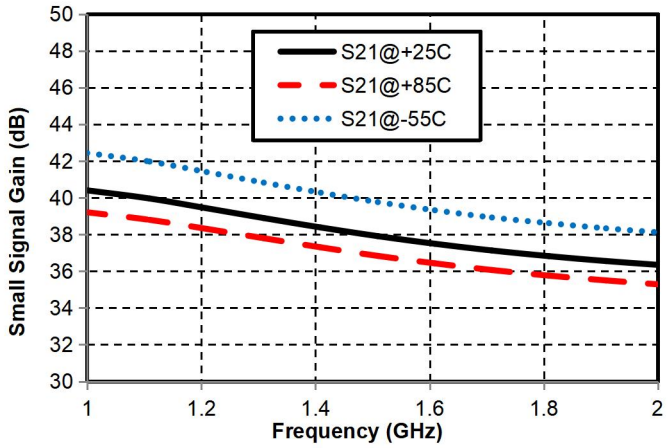
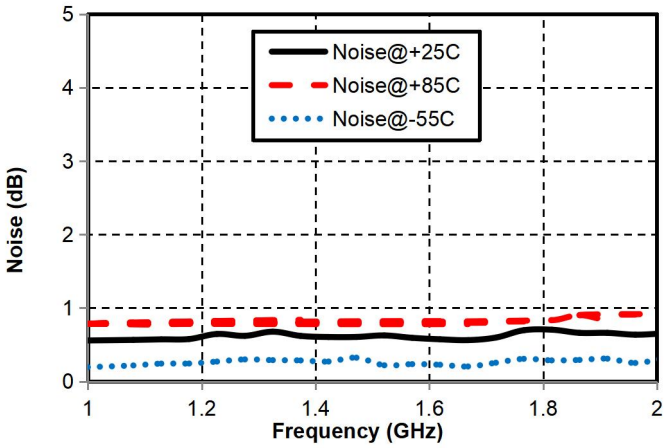
Main index test curve

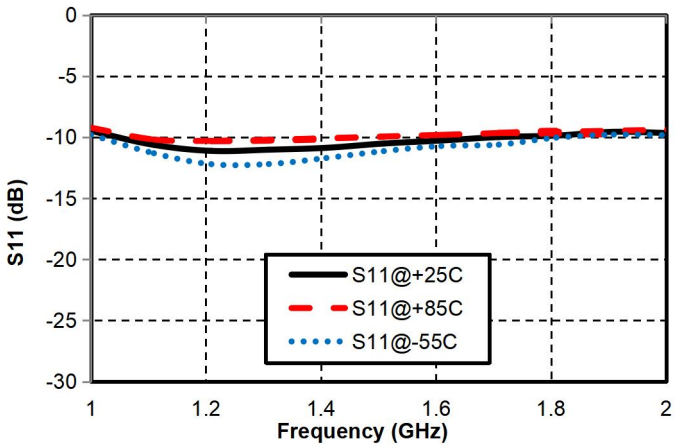
Gain vs. Frequency



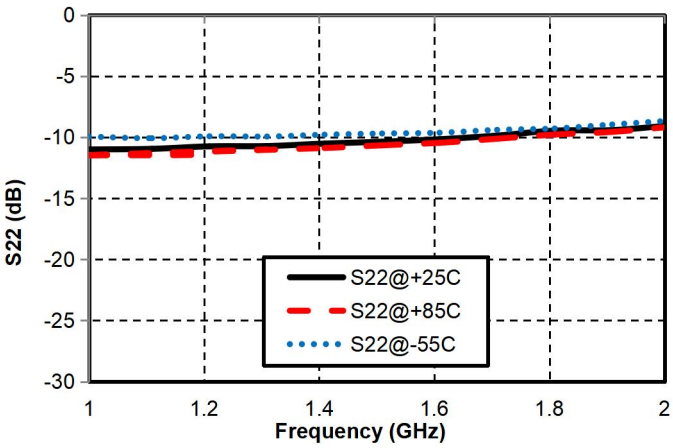
Noise Figure vs. Frequency



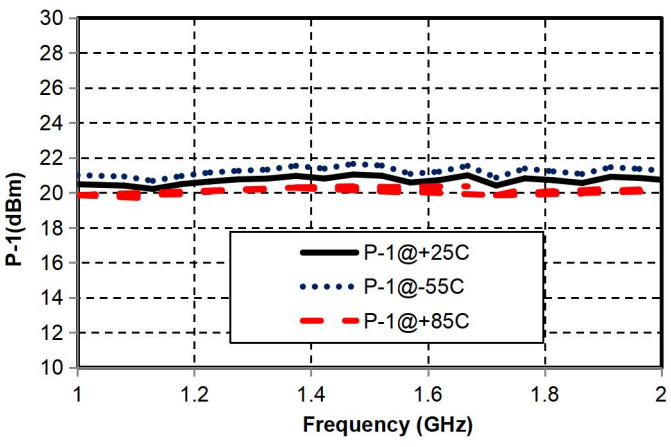
Input Return Loss vs. Frequency



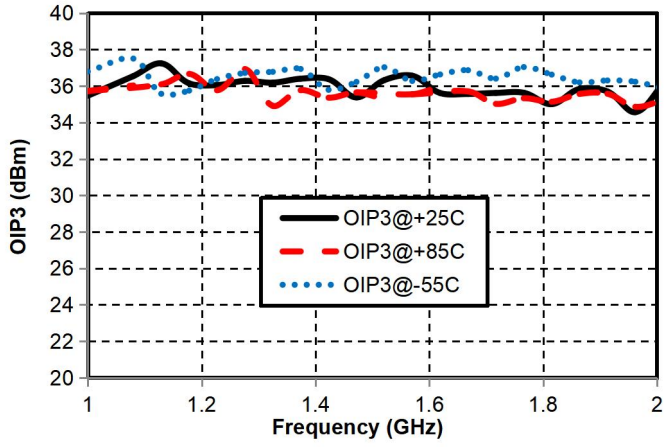
Output Return Loss vs. Frequency



P-1dB vs. Frequency



OIP3 vs. Frequency



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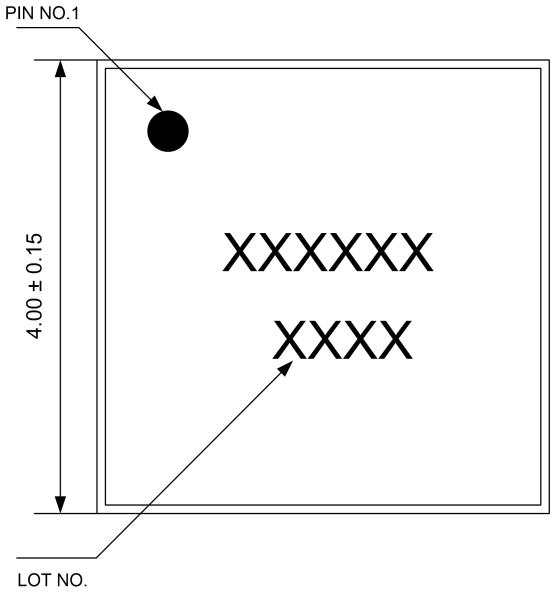
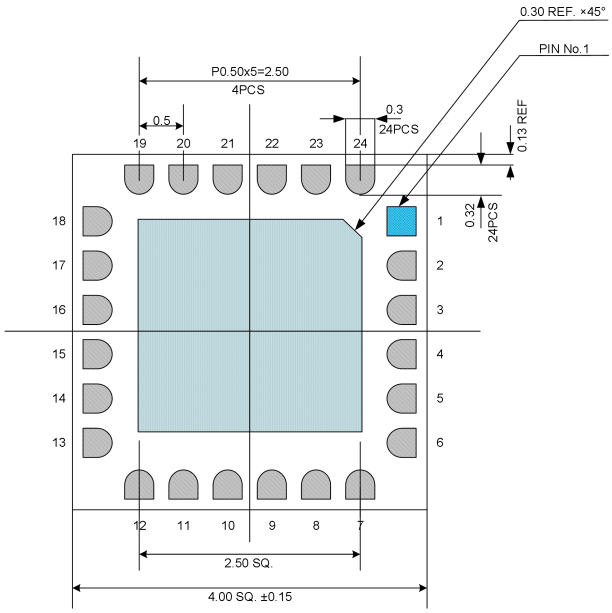
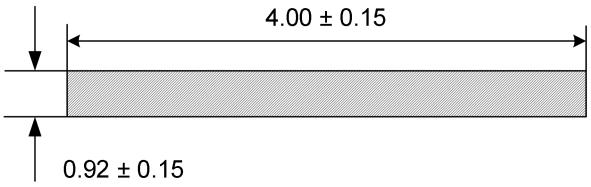
Appearance structure



Top view



Bottom view



Side View

The units in the figures are all in millimeters , and the tolerance is ±0.15 mm.

Pin Definition

Pin Definition	Function Symbol	Functional Description
3	RFIN 1	RF signal 1 input terminal, no DC blocking capacitor required
8	RFOUT1	RF signal 1 output terminal, no DC blocking capacitor required
11	RFIN 2	RF signal 2 input terminal, no DC blocking capacitor required
16	RFOUT2	RF signal 2 output terminal, no DC blocking capacitor required
23	VCC1	Amplifier U1 drain bias
20	VCC2	Amplifier U2 drain bias
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC
Other Ports	GND	No welding required, can be grounded

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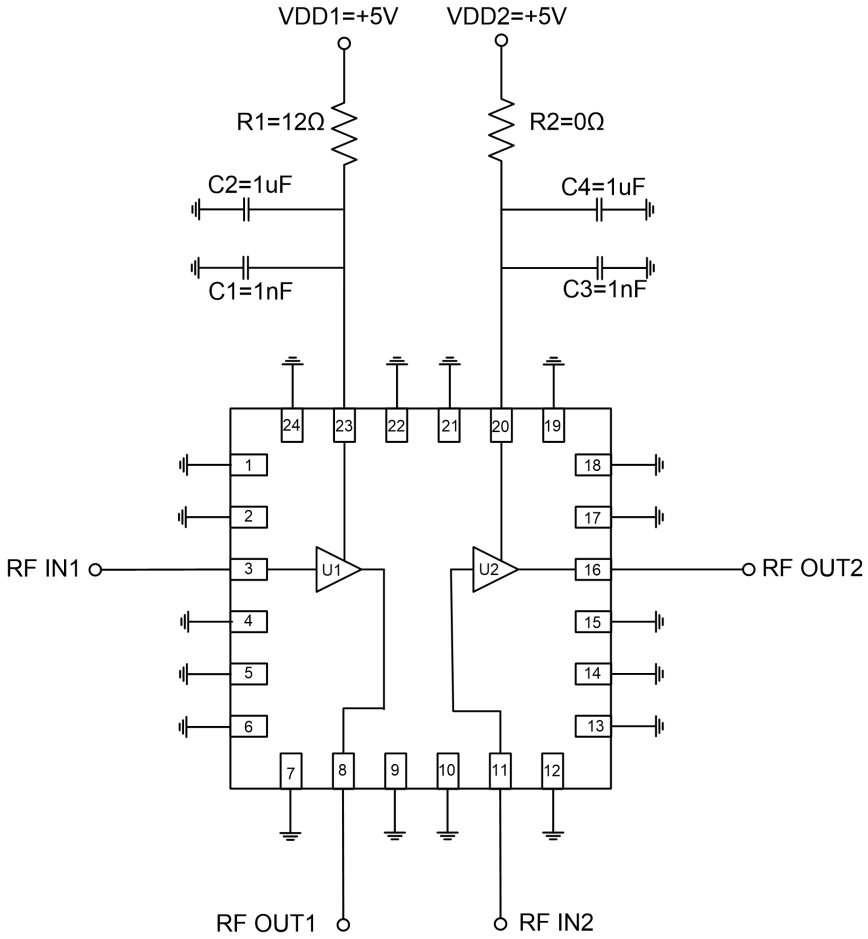
Recommended Circuit



*The U1 chip is GLA-012017A (XGLA7A1) and the U2 chip is GLA-012017B (XGLA7A 2).

Precautions for use

- Sealing material : Ceramic material that meets ROSH standards
- Lead surface plating: gold, gold layer thickness 0.30um MIN
- Maximum reflow peak temperature: 260 ℃

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