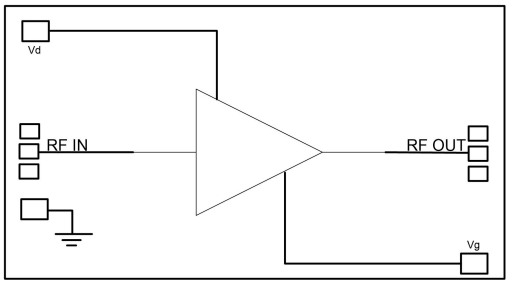
GLA-0020-2.0A

GaAs MMIC Low Noise Amplifier Chip，DC-20GHz

Performance characteristics

- Frequency range: DC-20GHz
- Small signal gain: 18dB
- Noise figure: 2.0dB typ./3.5dB max.
- P-1dB: 16dBm
- Power supply: +8V/80mA
- Input/Output: 50Ohm
- 100% on-chip testing
- Chip size: 3.3 x 1.6 x 0.1mm

Functional Block Diagram



Product Introduction

GLA-0020-2A is a broadband low-noise distributed amplifier chip, with a frequency range covering DC~20GHz, a small signal gain of 18dB, a P-1dB output power of 16dBm, and a typical noise figure of 2.0dB in the band. The GLA-0020-2A is powered by dual power sources of+8V and+0.65V. This product has no power on timing requirements.GLA-0020-2A can operate under+5V conditions, with a small signal gain of 18dB and an output power of 14dBm at P-1dB.

Use restriction parameters[1]	
Maximum leakage voltage	+12V
Maximum input power	+20dBm
Working temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of the above maximum limits may result in permanent damage.

Electrical performance parameters(T_A = +25°C，Vd=+8V)				
Index	Minimum value	Typical value	Maximum value	Unit
Frequency range		DC-20		GHz
Small signal gain	17.5	18	19	dB
Gain flatness		±0.75		dB
Noise figure	-	2.0	3.5	dB
P-1dB	15.5	16	17	dBm
Input return loss		22		dB
Output return Loss		20		dB
Static current		80		mA

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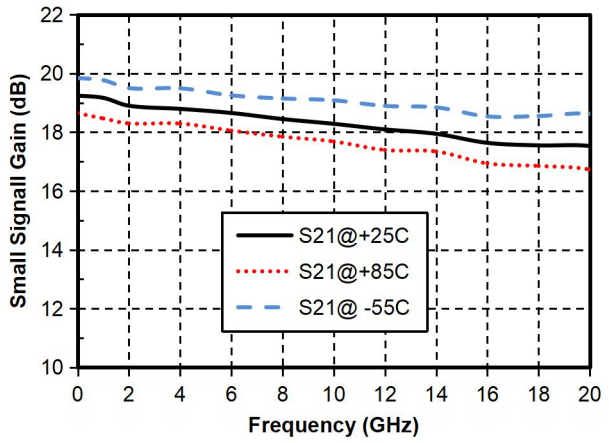
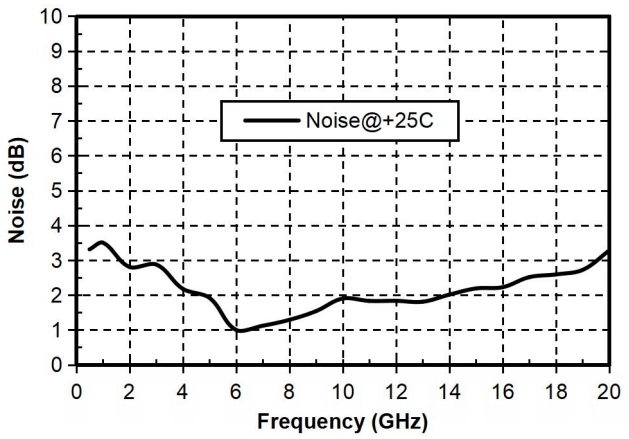
Main indicator testing curve

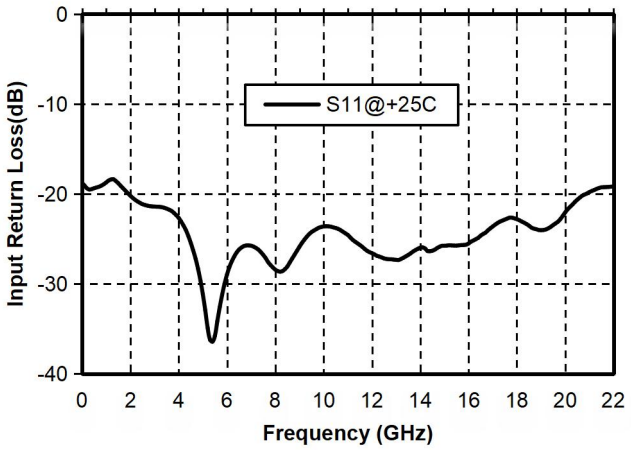
Gain vs. Temperature



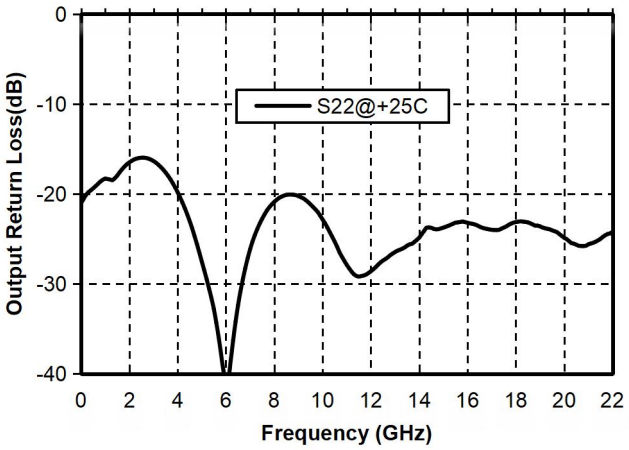
Noise Figure vs. Frequency



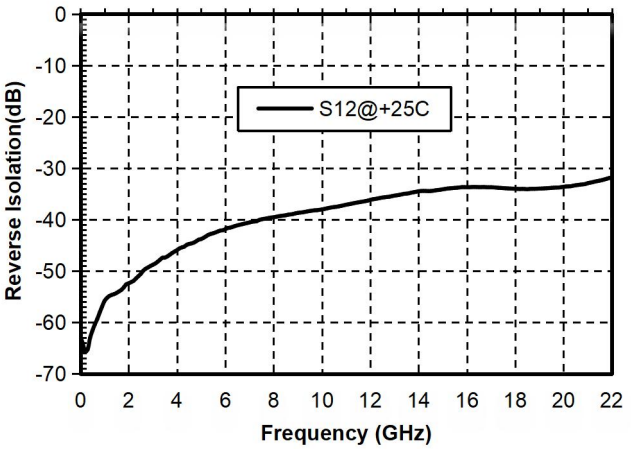
Input return loss vs. Frequency



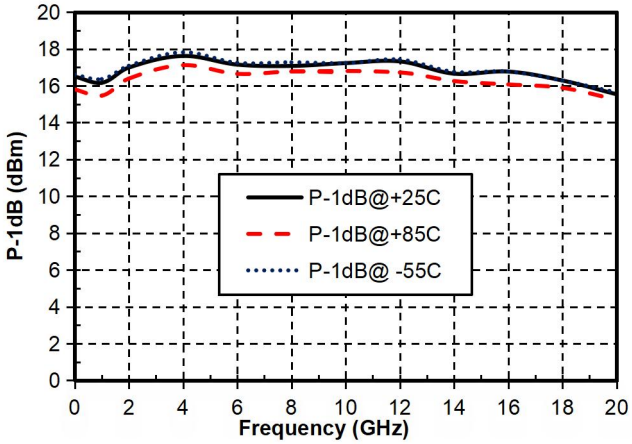
Output return Loss vs. Frequency



Reverse isolation vs. Frequency



P-1dB vs. Frequency



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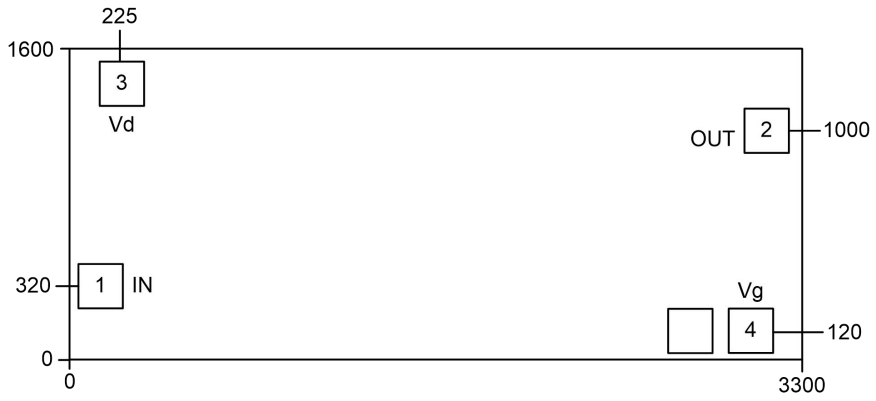
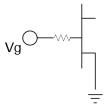
External structure[2]



【2】The units in the figure are all millimeters.

键合压点定义			
Bond point number	Functional symbols	Function Description	equivalent circuit
1	RF IN	RF signal input terminal requires a DC isolated capacitor.	
2	RF OUT	RF signal output terminal requires a DC isolated capacitor.	
3	VD	Amplifier drain bias, requires an external 100pF bypass capacitor.	
4	VG	Amplifier gate bias, requires external 100pF and 0.1uF bypass capacitors.	
Chip bottom	GND	The bottom of the chip needs to be well grounded with RF and DC.	

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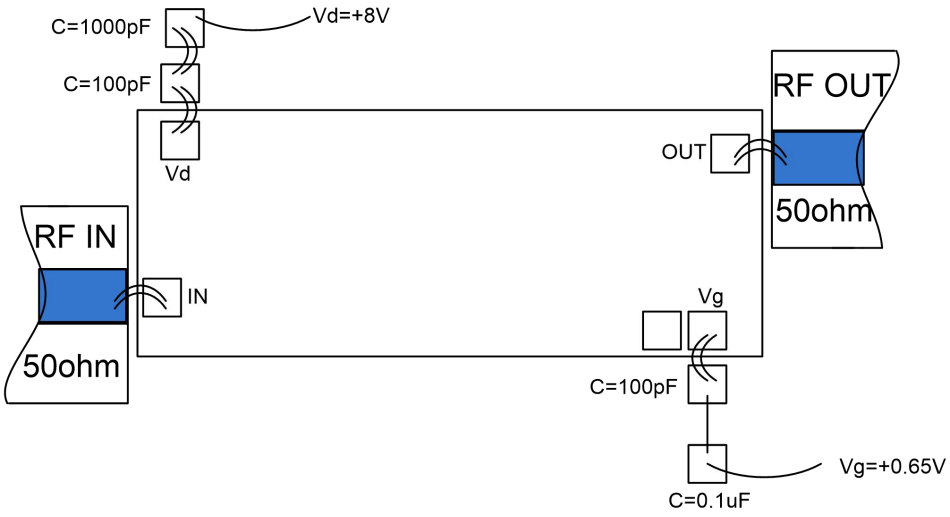
Recommended assembly diagram



Notice

- The chip needs to be stored in a container with anti-static function and stored in a nitrogen environment.
- Attempting to clean the surface of bare chips using wet chemical methods is prohibited.
- Please strictly comply with ESD protection requirements to avoid static damage to bare chips.
- Routine operation: Please use precision pointed tweezers to remove the bare chip. During the operation, avoid tools or fingers touching the surface of the chip.
- Suggestion for mounting operation: Bare chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold tin ratio of 80/20. The working surface temperature reached 255 ℃, and the tool (vacuum chuck) temperature reached 265 ℃. When a high-temperature mixed gas (nitrogen to hydrogen ratio of 90/10) is blown onto the chip, the temperature at the top of the tool should be raised to 290 ℃. Do not let the chip stay above 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive adhesive applied should be as small as possible. After placing the chip in the installation position, the conductive adhesive can be vaguely visible around it. Please follow the information provided by the conductive adhesive manufacturer for curing conditions.
- Suggestion for bonding operation: Both spherical or wedge-shaped bonding should be used Φ 0.025mm (1mil) gold wire. Thermal ultrasonic bonding temperature is 150 ℃. The pressure of the spherical bonding cutter is 40-50GF, and the pressure of the wedge bonding cutter is 18-22GF. Use as little ultrasonic energy as possible. The bonding process starts at the pressing point on the

chip and ends at the packaging (or substrate).